

N-Channel Enhancement Mode Field Effect Transistor

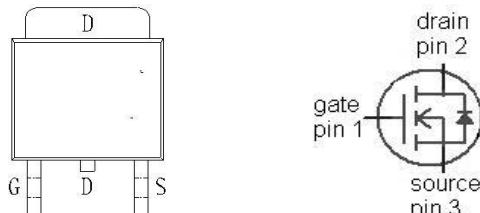
- Features

- Super Low Gate Charge
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

- Product Summary

V_{DS}	100	V
$R_{DS(on)}$	34	$\text{m}\Omega$
I_D	30	A

- Pin Configurations(TO252)



Top View

- Absolute Maximum Ratings

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current, $V_{GS}=10\text{V}^1$	I_D	8	A
		5.4	
		30	
		15	
Pulsed Drain Current ²	I_{DM}	40	
Avalanche Current	I_{AS}	20	
Single Pulse Avalanche Energy ³	E_{AS}	100	
Total Power Dissipation ³	P_D	2	W
		34.7	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C
Thermal Characteristics			
Parameter	Symbol	Max	Units
Thermal Resistance Junction-ambient ¹	$R_{\theta JA}$	62	°C/W
Thermal Resistance Junction-Case ¹	$R_{\theta JL}$	3.6	

FS30N10

- Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

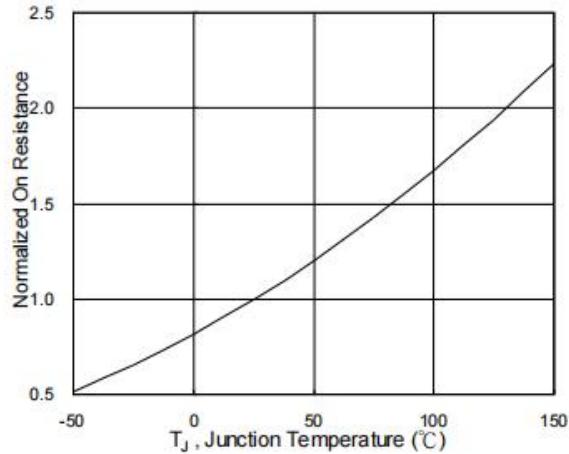
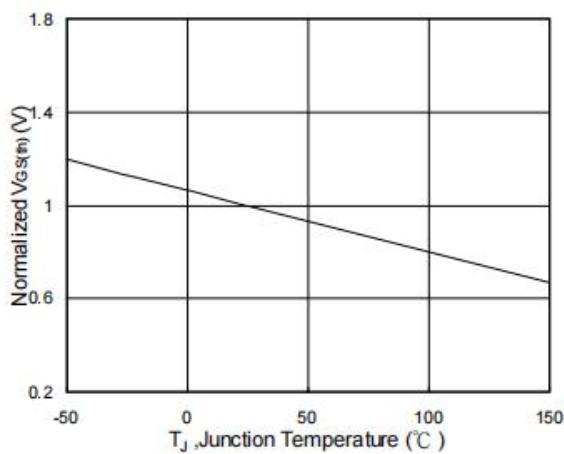
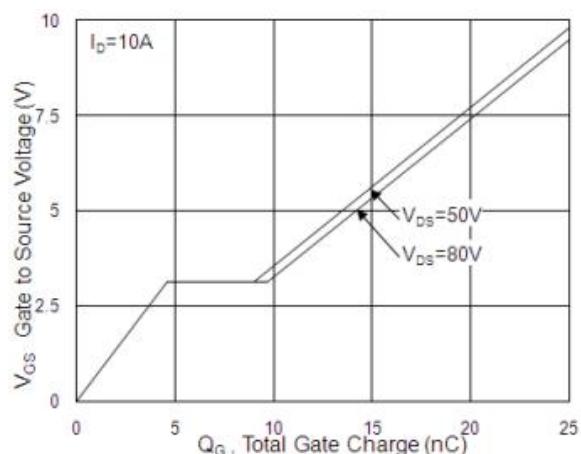
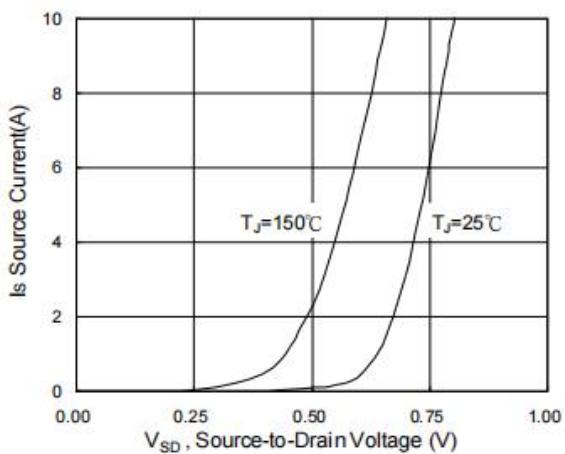
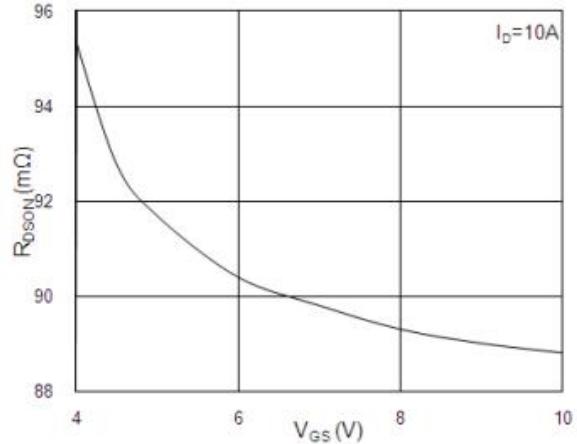
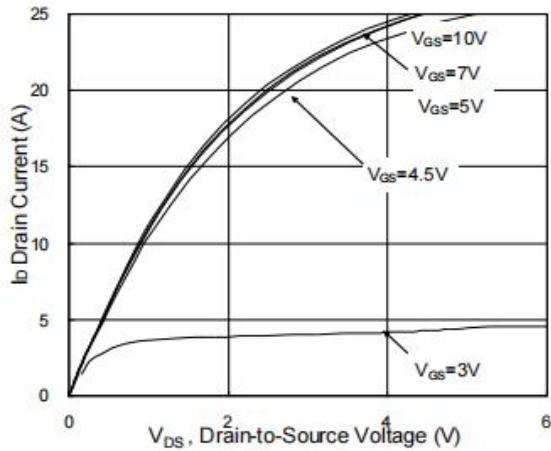
Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	100			V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=80\text{V}, V_{GS}=0$	$T_J=25^\circ\text{C}$		1	uA
			$T_J=55^\circ\text{C}$		5	
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 0.1	
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1		2.5	V
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{GS}=10\text{V}, I_D=10\text{A}$		34	40	mΩ
				40	50	
g_{FS}	Forward Trans conductance	$V_{DS}=5\text{V}, I_D=10\text{A}$		13		S
V_{SD}	Diode Forward Voltage ²	$I_S=1\text{A}, V_{GS}=0\text{V}, T_J=25^\circ\text{C}$			1.2	V
I_{SM}	Pulsed Source Current ^{2,5}	$V_G=V_D=0\text{V}, \text{Force Current}$			35	A
					30	
C_{iss}	Input capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1\text{MHz}$		1535		pF
C_{oss}	Output capacitance			60		
C_{rss}	Reverse transfer capacitance			37		
Q_g	Total Gate Charge(10V)	$V_{GS}=10\text{V}, V_{DS}=80\text{V}, I_D=10\text{A}$		26.2		nC
Q_{gs}	Gate - Source Charge			4.6		
Q_{gd}	Gate - Drain Charge			5.1		
R_g	Gate resistance	$V_{DS}=0\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$		2		Ω
$t_{D(\text{on})}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DD}=50\text{V}, R_G=3.3\Omega, I_D=10\text{A}$		4.2		ns
t_r	Turn-On Rise Time			8.2		
$t_{D(\text{off})}$	Turn-Off Delay Time			35.6		
t_f	Turn-Off Fall Time			9.6		
t_{rr}	Body Diode Reverse Recovery Time	$I_F=10\text{A}, dI/dt=100\text{A}/\mu\text{s}, T_J=25^\circ\text{C}$		37		

Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is $V_{DD}=25\text{V}, V_{GS}=10\text{V}, L=0.1\text{mH}, I_{AS}=11\text{A}$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

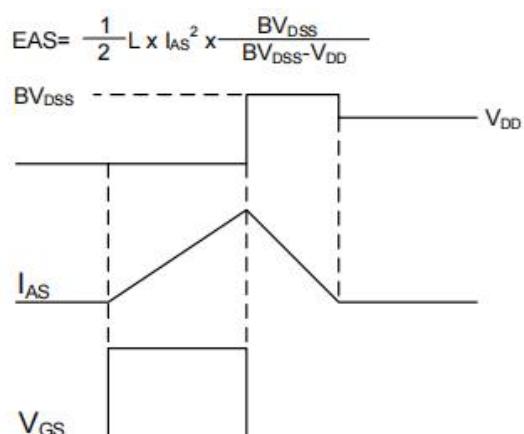
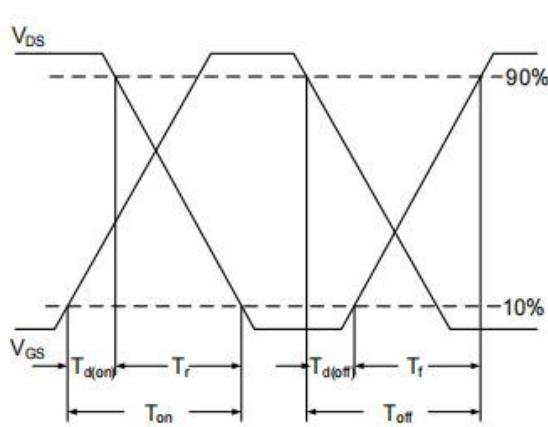
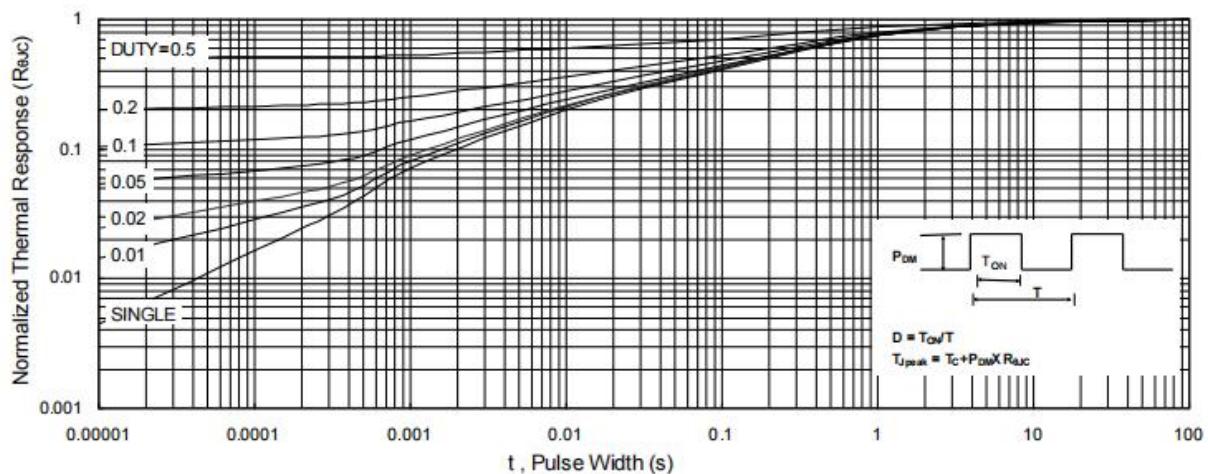
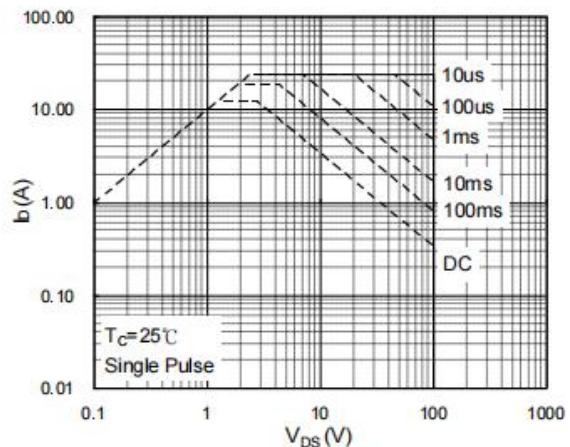
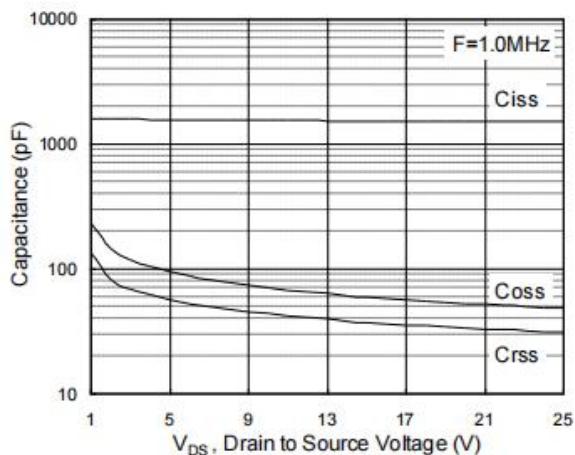
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- TYPICAL CHARACTERISTICS



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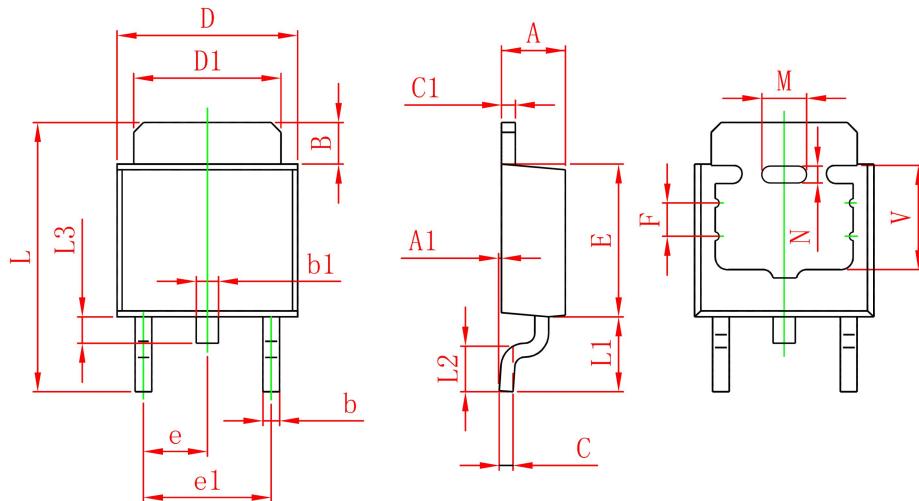
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- Package Information

TO-252C-2L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
F	1.200REF.		0.047REF.	
M	1.600REF.		0.063REF.	
N	0.450REF.		0.018REF.	
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.600	0.900	0.024	0.035
V	3.800 REF		0.150 REF	