

N-Channel 30-V (D-S) MOSFET

● FEATURES

$R_{DS(ON)} \leq 7.5m\Omega @ V_{GS}=10V$

$R_{DS(ON)} \leq 10m\Omega @ V_{GS}=4.5V$

high density cell design for extremely low $R_{DS(ON)}$

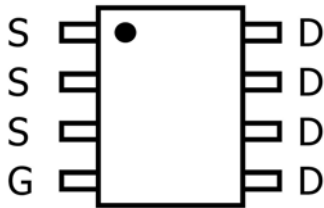
Exceptional on-resistance and maximum DC current capability

● GENERAL DESCRIPTION

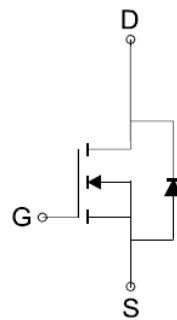
The FS73A3B combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

This device is ideal for load switch and battery protection applications.

● PIN CONFIGURATION



SOP8



N-Channel MOSFET

● Absolute Maximum Ratings ($T_A=25^\circ C$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Units
Drain-Source Voltage	VDS	30	V
Gate-Source Voltage	VGS	± 20	V
Drain Current-Continuous	ID	65	A
Drain Current-Pulsed a	IDM	200	A
Maximum Power Dissipation @ $T_C = 25^\circ C$ -Derate above $25^\circ C$	PD	78	W
		0.53	W/ $^\circ C$
Single Pulsed Avalanche Energy ^d	EAS	160	mJ
Single Pulsed Avalanche Current ^d	IAS	25	A
Operating and Store Temperature Range	TJ, Tstg	-55 to 175	C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	RqJC	1.9	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	RqJA	62.5	$^\circ C/W$

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● Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V, ID=250μA	30			V
VGS(th)	Gate Threshold Voltage ^b	VDS=VGS, ID=250μA	1.3	1.8	3	V
IGSS	Gate Leakage Current	VDS=0V, VGS=±20V			±100	nA
IDSS	Zero Gate Voltage Drain Current	VDS=30V, VGS=0V			1	μA
RDS(ON)	Drain-Source On-State Resistance ^a	VGS=10V, ID= 50A		7.5	9	mΩ
		VGS=4.5V, ID= 40A		10	12	
VSD	Diode Forward Voltage	IS=2.7A, VGS=0V		0.72	1.1	V
DYNAMIC ^c						
Qg	Total Gate Charge(10V)	VDS=15V, VGS=10V, ID=17A		55		nC
Qg	Total Gate Charge(4.5V)	VDS=15V, VGS=4.5V, ID=17A		29		
Qgs	Gate-Source Charge			10		
Qgd	Gate-Drain Charge			15		
Ciss	Input capacitance	VDS=15V, VGS=0V, f=1.0MHz		3400		pF
Coss	Output Capacitance			550		
Crss	Reverse Transfer Capacitance			210		
Rg	Gate-Resistance	VDS=0V, VGS=0V, f=1MHz		1.2		Ω
td(on)	Turn-On Delay Time	VDD=15V, RL =15Ω ID=1A, VGEN=10V RG=6Ω		23		ns
tr	Turn-On Rise Time			12		
td(off)	Turn-Off Delay Time			86		
tf	Turn-Off Fall Time			12		

Note:

a: Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%

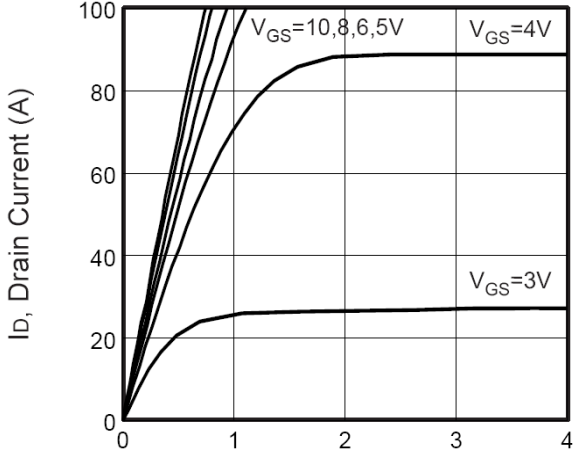
b: FORSEMI reserves the right to improve product design, functions and reliability without notice.

c. Guaranteed by design, not subject to production testing.

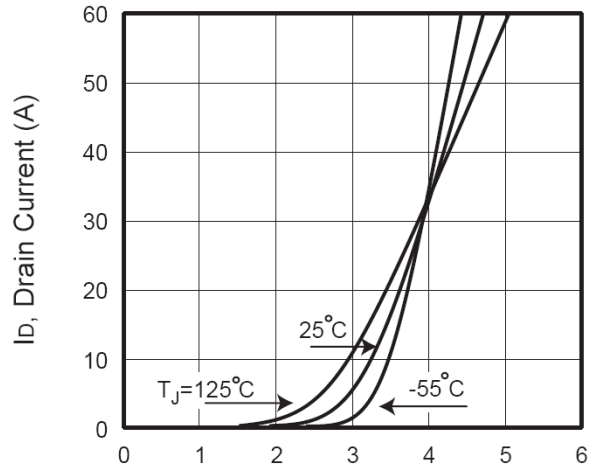
d. L = 0.5mH, IAS = 35A, VDD = 24V, RG = 25Ω, Starting T_J = 25°C

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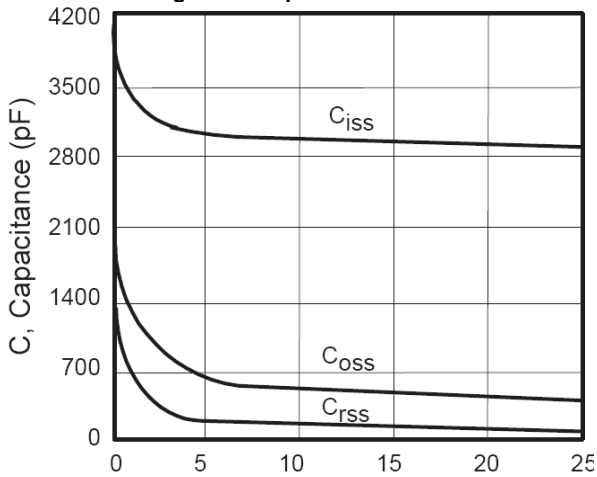
● **Typical Performance Characteristics (T = 25°C)**



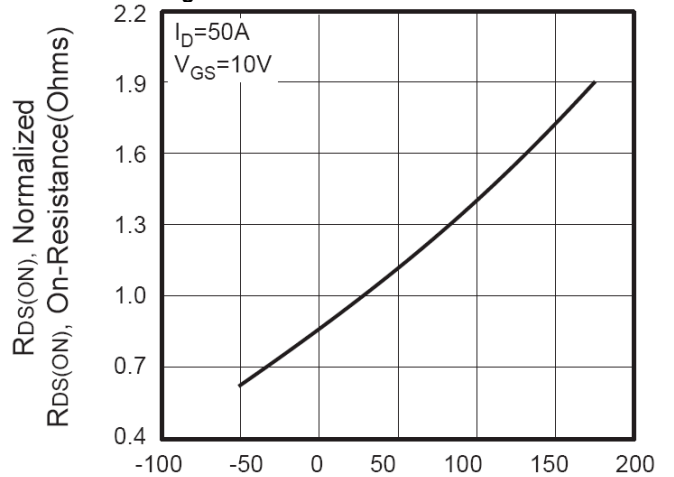
V_{DS} , Drain-to-Source Voltage (V)
Figure 1. Output Characteristics



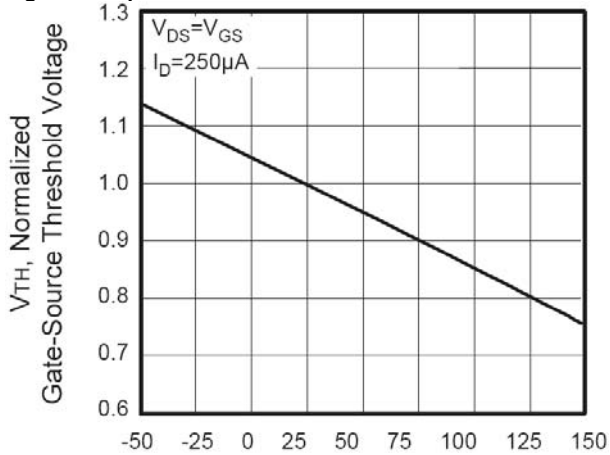
V_{GS} , Gate-to-Source Voltage (V)
Figure 2. Transfer Characteristics



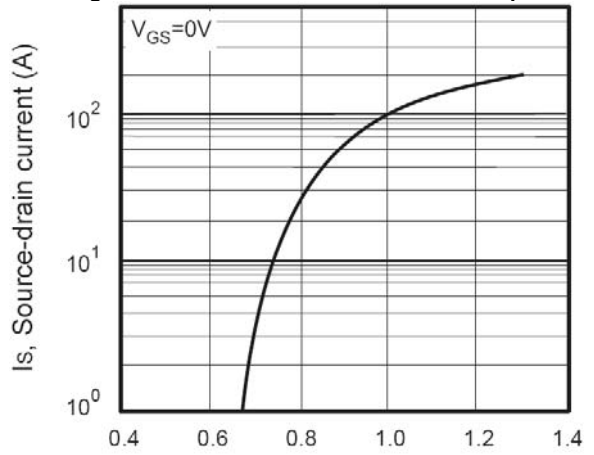
V_{DS} , Drain-to-Source Voltage (V)
Figure 3. Capacitance



T_J , Junction Temperature(°C)
Figure 4. On-Resistance Variation with Temperature

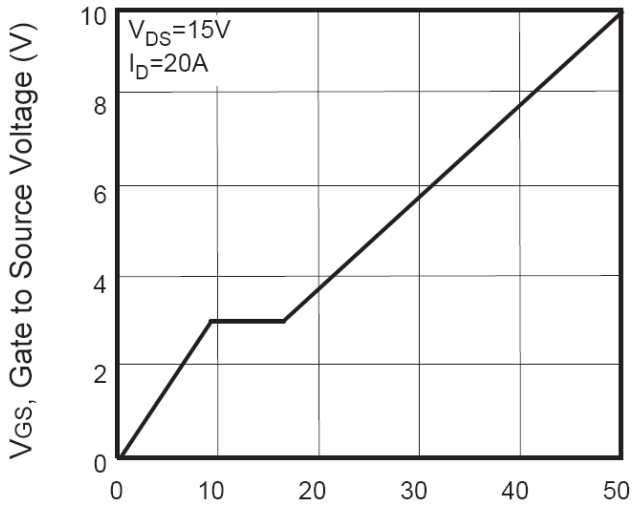


T_J , Junction Temperature(°C)
Figure 5. Gate Threshold Variation with Temperature

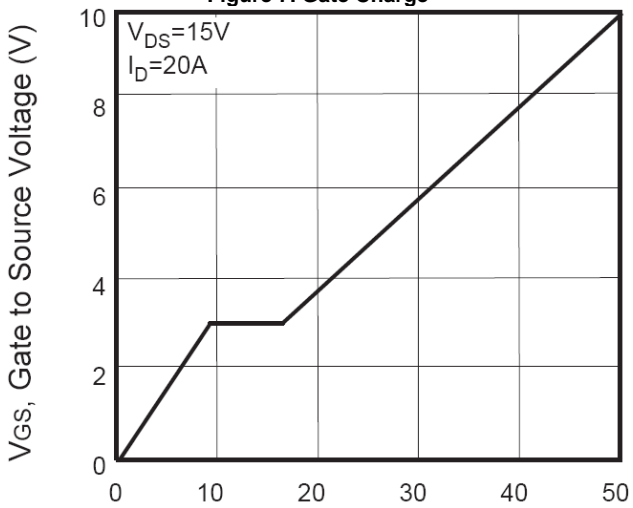


V_{SD} , Body Diode Forward Voltage (V)
Figure 6. Body Diode Forward Voltage Variation with Source Current

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Qg, Total Gate Charge (nC)
Figure 7. Gate Charge



Qg, Total Gate Charge (nC)
Figure 7. Gate Charge

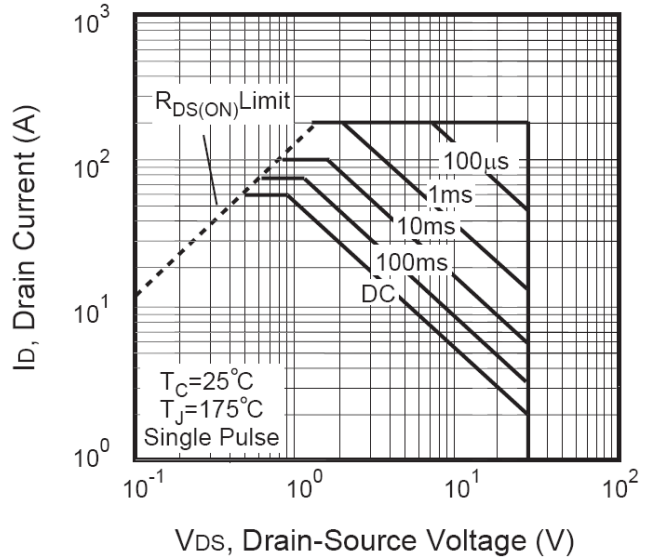


Figure 8. Maximum Safe Operating Area

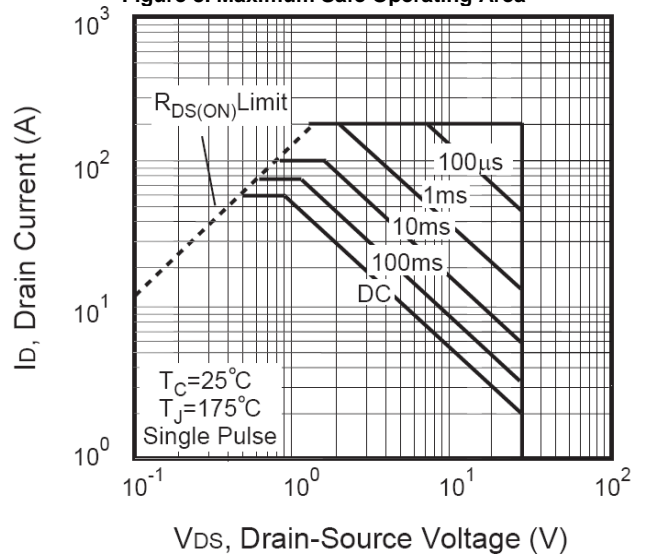
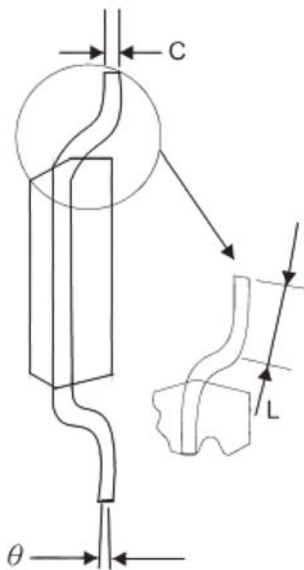
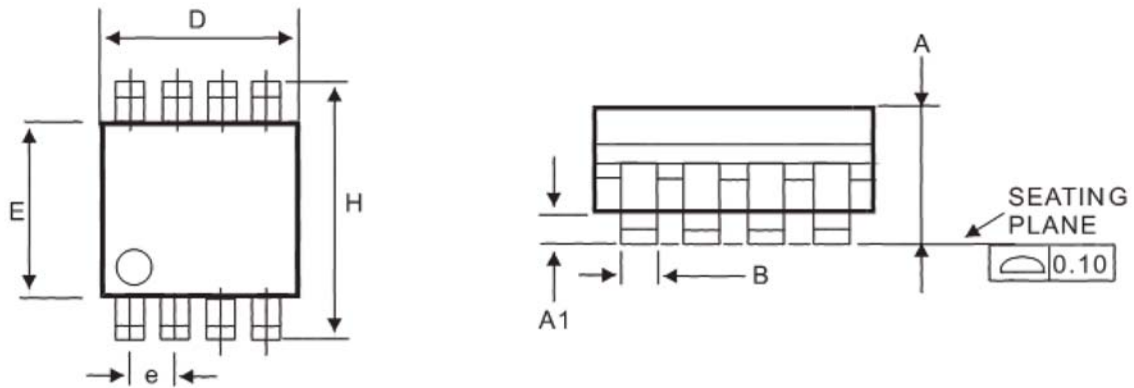


Figure 8. Maximum Safe Operating Area

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- PACKAGE

SOP-8 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.