

## DUAL N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

- Features**

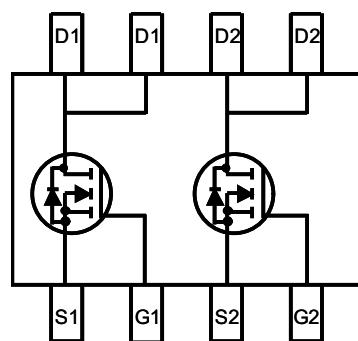
Advanced trench process technology  
 High Density Cell Design For Ultra Low On-Resistance  
 High Power and Current handing capability  
 Fully Characterized Avalanche Voltage and Current

- General Description**

Case: SOP8  
 Case Material: Molded Plastic. UL Flammability Classification  
 Rating 94V-0  
 Moisture Sensitivity: Level 1 per J-STD-020C  
 Terminals: Solderable per MIL-STD-202, Method 208

- Pin configurations**

See Diagram below



- Maximum Ratings @  $T_A = 25^\circ\text{C}$  unless otherwise specified**

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		$V_{DSS}$	20	V
Gate-Source Voltage		$V_{GSS}$	$\pm 12$	
Drain Current (Note 1)	Continuous	$I_D$	3.7	A
	Pulsed		6	
Total Power Dissipation (Note 1)		$P_D$	0.69	W
Operating and Storage Temperature Range		$T_J, T_{STG}$	-55 to +150	°C

Note: 1. Mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch, for each singlate die, the  $P_D$  is 75%.

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- **Electrical Characteristics** @  $T_A = 25^\circ\text{C}$  unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS (Note 2)</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	20	--	--	V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}} = 20\text{V}, V_{\text{GS}} = 0\text{V}$	--	--	1	$\mu\text{A}$
Gate-Body Leakage	$I_{\text{GSS}}$	$V_{\text{GS}} = \pm 12\text{V}, V_{\text{DS}} = 0\text{V}$	--	--	$\pm 100$	nA
<b>ON CHARACTERISTICS (Note 2)</b>						
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	0.6	--	--	V
Static Drain-Source On-Resistance	$R_{\text{DS(ON)}}$	$V_{\text{GS}} = 4.5\text{V}, I_D = 6\text{A}$	--	25	50	$\text{m}\Omega$
		$V_{\text{GS}} = 2.5\text{V}, I_D = 5.2\text{A}$	--	34	65	
Forward Transconductance	$g_{\text{fs}}$	$V_{\text{DS}} = 10\text{V}, I_D = 6\text{A}$	--	5	--	S
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}} = 10\text{V}, V_{\text{GS}} = 0\text{V}$ $f = 1.0\text{MHz}$	--	562	--	$\text{pF}$
Output Capacitance	$C_{\text{oss}}$		--	79	--	
Reverse Transfer Capacitance	$C_{\text{rss}}$		--	73	--	
Total Gate Charge	$Q_g$	$V_{\text{DS}} = 10\text{V}, I_D = 6\text{A},$ $V_{\text{GS}} = 4.5\text{V}$	--	4.86	--	$\text{nC}$
Gate-Source Charge	$Q_{\text{gs}}$		--	0.92	--	
Gate-Drain	$Q_{\text{gd}}$		--	1.4	--	
<b>SWITCHING CHARACTERISTICS</b>						
Turn-On Delay Time	$t_{\text{D(ON)}}$	$V_{\text{DD}} = 10\text{V}, I_D = 1\text{A},$ $V_{\text{GEN}} = 4.5\text{V}, R_G = 6\Omega$	--	18	--	$\text{ns}$
Turn-Off Delay Time	$t_{\text{D(OFF)}}$		--	25	--	

Note: 2. Short duration test pulse used to minimize self-heating effect.

- Typical Performance Characteristics

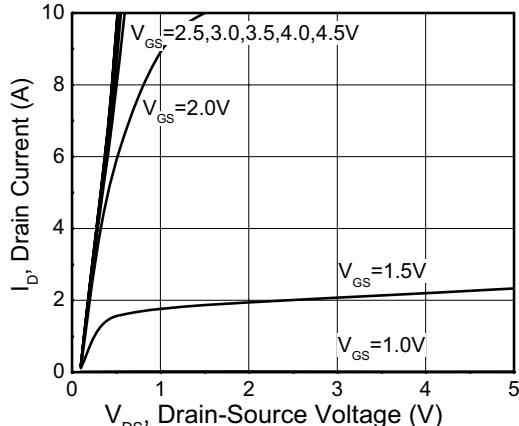


Figure 1. Output Characteristics

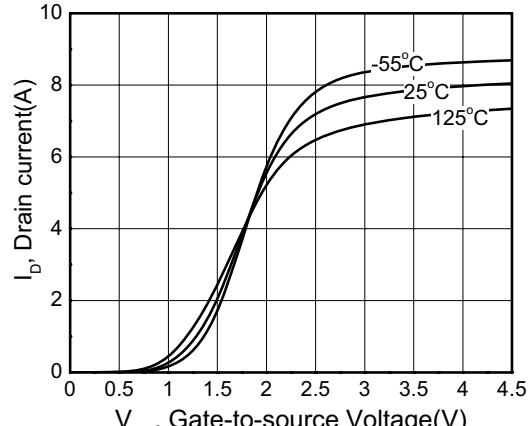


Figure 2. Transfer Characteristics

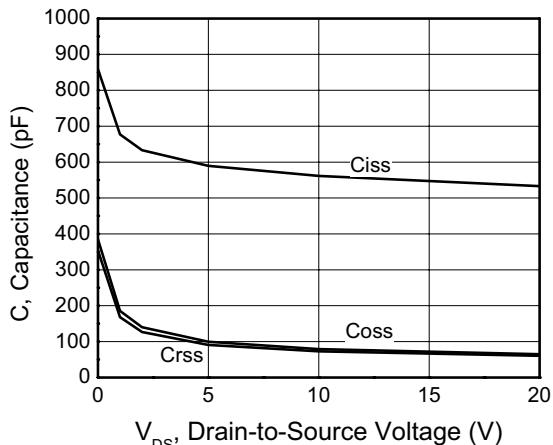


Figure 3. Capacitance

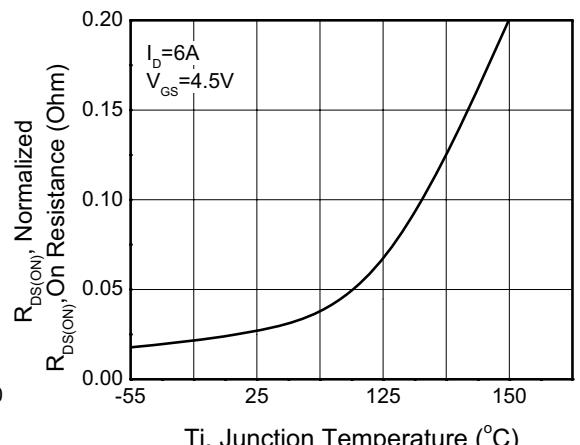


Figure 4. On Resistance Vs. Temperature

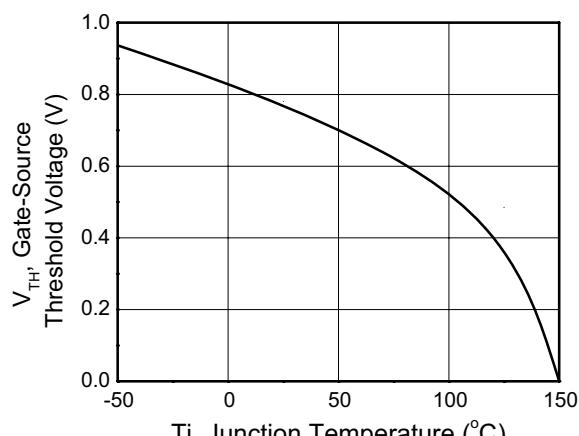


Figure 5. Gate Threshold Vs. Temperature

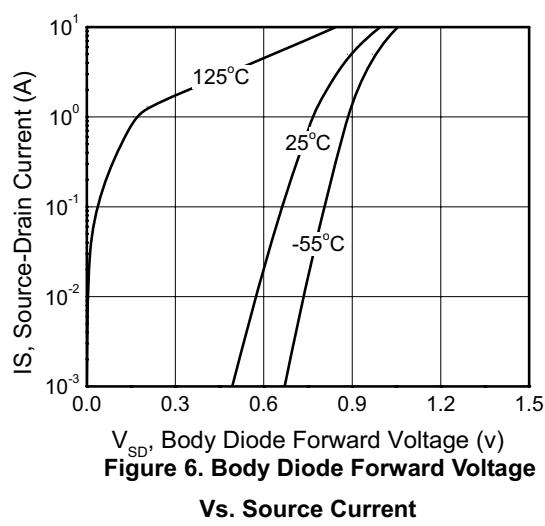
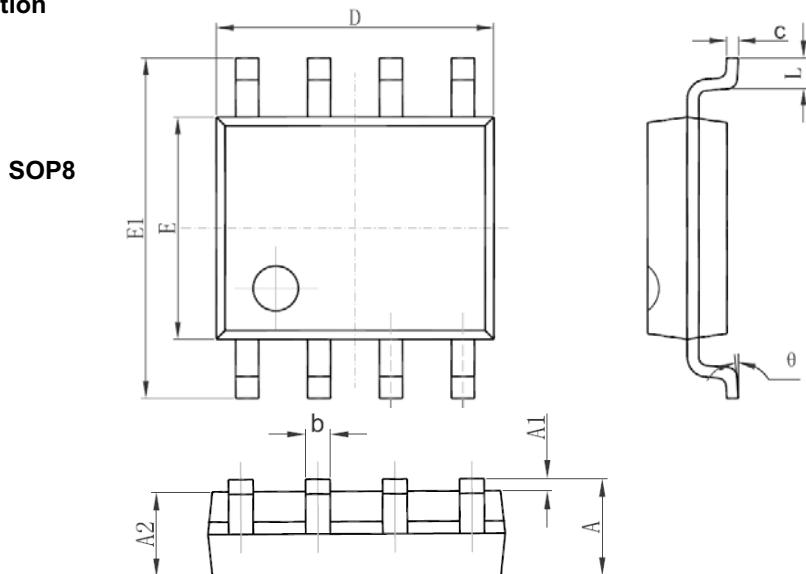


Figure 6. Body Diode Forward Voltage

Vs. Source Current

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- Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°