# N-mos With Gate Protect Diode

## Features

20V/6.5A, RDS(ON)=20 mΩ@VGS=4.5V

20V/5.5A, RDS(ON)=23 mΩ@VGS=2.5V

20V/5A, RDS(ON)=30 mΩ@VGS=1.8V

Super high density cell design for extremely low RDS(ON)

Exceptional on-resistance and maximum DC current Capability

## APPLICATIONS

Power Management in Note book

Portable Equipment

DC/DC Converter

Load Switch

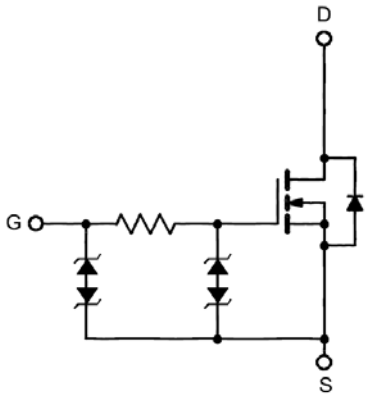
DSC

LCD Display inverter

## General Description

The FS2312D is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

## Pin Configurations




## Absolute Maximum Ratings @$T_A$=25℃ unless otherwise noted

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | VDSS | 20 | V |
| Gate-Source Voltage | | VGSS | ±8 | V |
| Continuous Drain Current(tJ=150℃) | TA=25℃ | ID | 6.5 | A |
| | TA=70℃ | | 5.2 | |
| Pulsed Drain Current | | IDM | 30 | A |
| Continuous Source Current (Diode Conduction) | | IS | 2.5 | A |
| Maximum Power Dissipation | TA=25℃ | PD | 1.4 | W |
| | TA=70℃ | | 0.9 | |
| Operating Junction Temperature | | TJ | -55 to 150 | ℃ |
| Storage Temperature Range | | Tstg | -55 to 150 | ℃ |
| Thermal Resistance-Junction to Ambient | | RθJA | 125 | ℃/W |

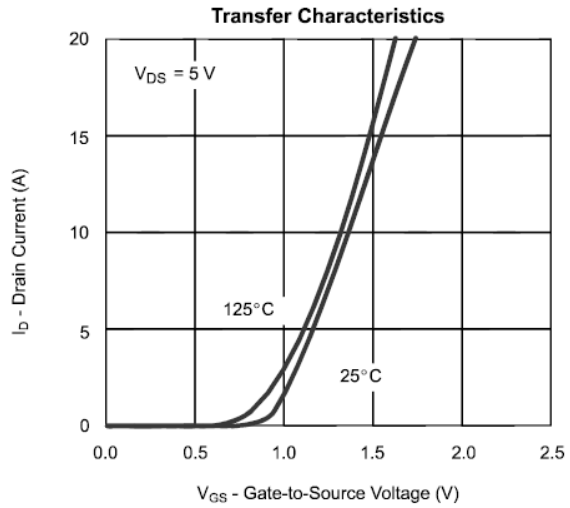
- **Electrical Characteristics** @TA=25℃ unless otherwise noted

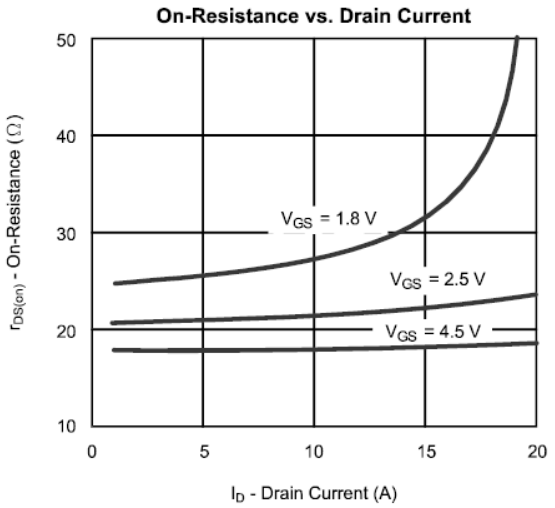
| Symbol | Parameter | Limit | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| V(BR)DSS | Drain-Source Breakdown Voltage | VGS=0V, ID=250μA | 20 | | | V |
| VGS(th) | Gate Threshold Voltage | VDS=VGS, ID=250μA | 0.4 | 0.6 | 1 | V |
| IGSS | Gate Leakage Current | VDS=0V, VGS=±4.5V | | | ±1 | nA |
| | | VDS=0V, VGS=±8V | | | ±10 | |
| IDSS | Zero Gate Voltage Drain Current | VDS=24V, VGS=0V | | | 1 | μA |
| | | VDS=16V, VGS=0V TJ=55℃ | | | 1 | |
| | | | | | 5 | |
| ID(ON) | On-State Drain Current | VDS=4.5V, VGS= 5V | 30 | | | A |
| RDS(ON) | Drain-Source On-Resistance | VGS=4.5V, ID= 6.5A | | 16 | 20 | mΩ |
| | | VGS=2.5V, ID= 5.5A | | 20 | 23 | |
| | | VGS=1.8V, ID= 5A | | 25 | 30 | |
| GFS | Forward Transconductance | VDS=5V, ID=6.5A | | 13 | | S |
| VSD | Diode Forward Voltage | IS=1A, VGS=0V | | 0.6 | 1 | V |
| **Dynamic** | | | | | | |
| Qg | Total Gate Charge | VDS=10V, VGS=4.5V, ID=6.5A | | 10 | | nC |
| Qgs | Gate-Source Charge | | | 1.4 | | |
| Qgd | Gate-Drain Charge | | | 2.7 | | |
| Ciss | Input Capacitance | VDS=10V, VGS=0V, f=1MHz | | 1100 | | pF |
| Coss | Output Capacitance | | | 104 | | |
| Crss | Reverse Transfer Capacitance | | | 29 | | |
| Rg | Gate resistance | VDS=10V, VGS=0V, f=1MH | | 1.5 | | Ω |
| td(on) | Turn-On Time | VDS=10V, RL= 1.5Ω VGS=5V, RGEN=3Ω | | 6.2 | | ns |
| tr | | | | 12.7 | | |
| td(off) | Turn-Off Time | | | 51.7 | | |
| tf | | | | 16 | | |

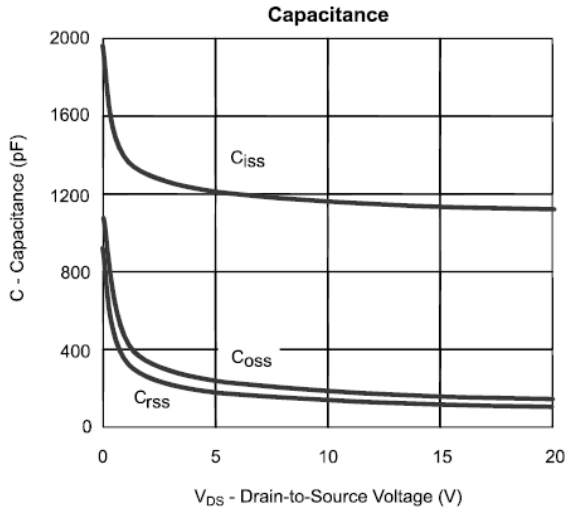
Notes:

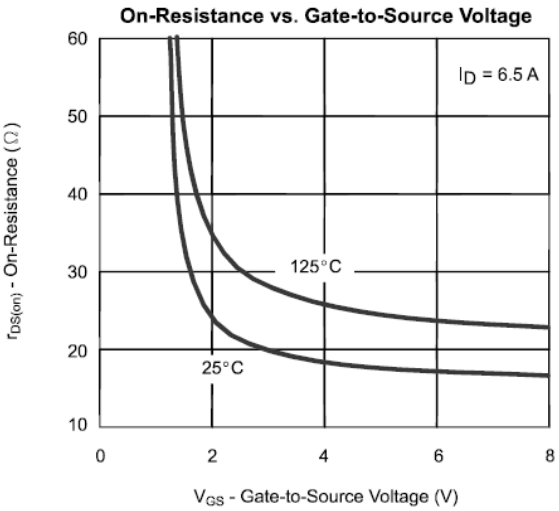
1. Pulse width limited by maximum junction temperature. Pulse test: PW≤300μs, duty cycle≤2%.
2. For design AID only, not subject to production testing. Switching time is essentially independent of operating temperature.

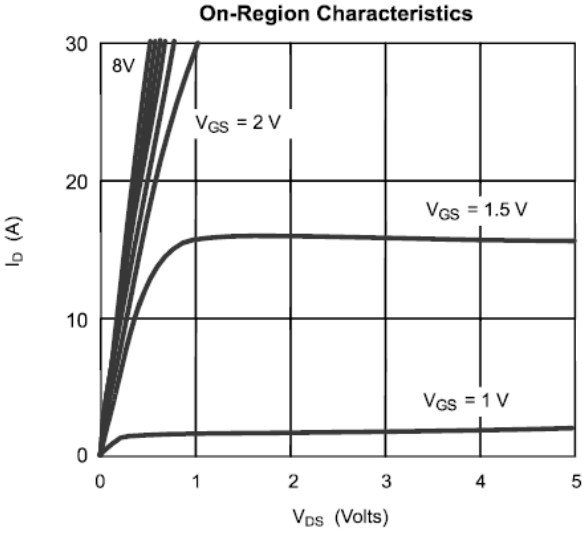
- **Typical Performance Characteristics**



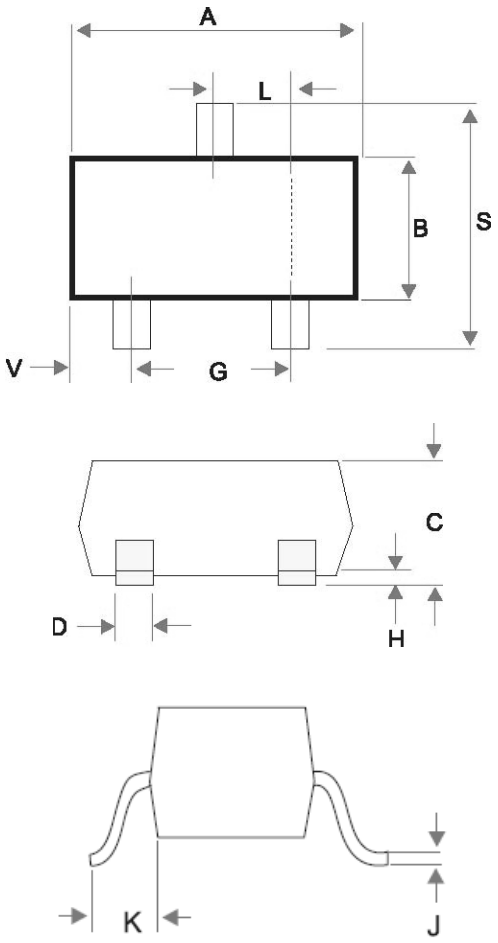



- Package Information

## SOT-23 Package Outline




| DIM | MILLIMETERS | |
|---|---|---|
| | MIN | MAX |
| A | 2.80 | 3.1 |
| B | 1.20 | 1.7 |
| C | 0.89 | 1.3 |
| D | 0.37 | 0.50 |
| G | 1.78 | 2.04 |
| H | 0.013 | 0.15 |
| J | 0.085 | 0.2 |
| K | 0.45 | 0.7 |
| L | 0.89 | 1.02 |
| S | 2.10 | 3 |
| V | 0.45 | 0.60 |