N-Channel Enhancement Mode Field Effect Transistor

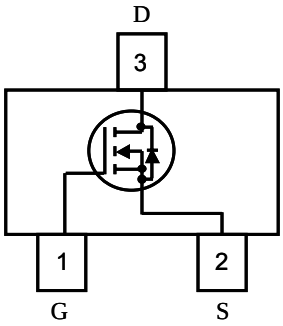
Features

Advanced trench process technology
High-density cell design for ultra low on-resistance
Compact and low profile SOT23 package

General Description

This N-Channel enhancement mode power FETs are produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage application such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package. Excellent thermal and electrical capabilities.

Pin Configurations



SOT23

Absolute Maximum Ratings @T_A=25℃ unless otherwise noted

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	Continuous	I_D	2.7	A
	Pulsed		10	
Power Dissipation		P_D	350	mW
Operating and Storage Junction Temperature Range		T_J, T_{STG}	-55 to +150	°C

- Electrical Characteristics @T_A=25℃ unless otherwise noted

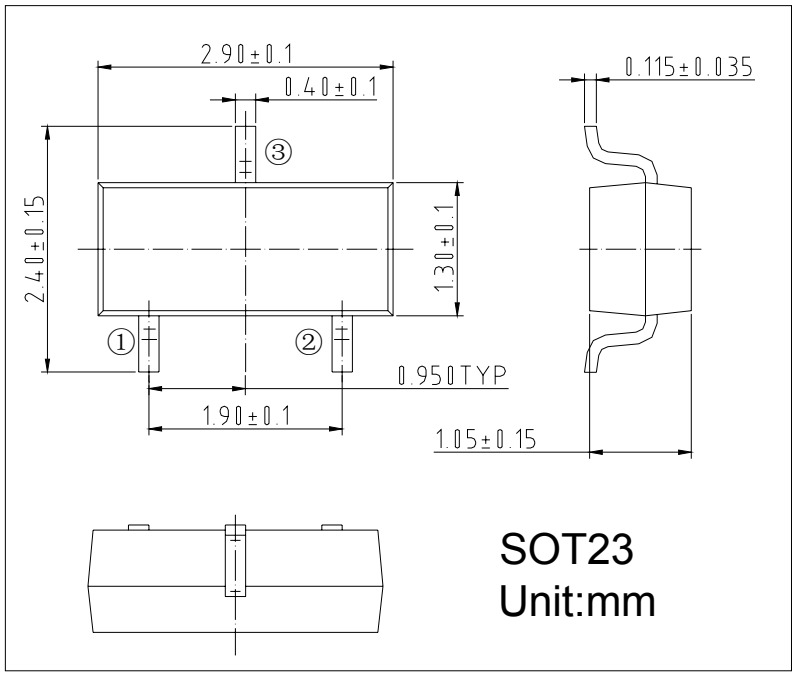
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
VDS	Drain-Source Breakdown Voltage	VGS=0V, ID=250μA	60			V
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=250μA	1.0		3.0	V
IGSS	Gate Leakage Current	VDS=0V, VGS=±20V			±100	nA
IDSS	Zero Gate Voltage Drain Current	VDS=60V, VGS=0V			1	μA
RDS(ON)	Drain-Source On-Resistancea	VGS=10V, ID= 2.6A		82	100	mΩ
		VGS=4.5V, ID= 2.1A		96	130	
		VGS=3.3V, ID= 1.8A		139	200	
VSD	Diode Forward Voltage	IS=1A, VGS=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	VDS=30V, VGS=10V, ID=2.6A		12		nC
Qg	Total Gate Charge	VDS=30V, VGS=4.5V, ID=2.6A		6.5		
Qgs	Gate-Source Charge			2.2		
Qgd	Gate-Drain Charge			2.7		
Ciss	Input capacitance	VDS=30V, VGS=0V, f=1.0MHz		350		pF
Coss	Output Capacitance			40		
Crss	Reverse Transfer Capacitance			12		
Rg	Gate Resistance	VDS=0V, VGS=0V, f=1MHz		0.7		Ω
td(on)	Turn-On Delay Time	VDD=20V, RL =20Ω ID=1A, VGEN=10V RG=1Ω		10		ns
tr	Turn-On Rise Time			11		
td(off)	Turn-Off Delay Time			29		
tf	Turn-Off Fall Time			3		

Notes :

(1).Pulse Test : Pulse Width < 300μs, Duty Cycle < 2%.

(2).Surface Mounted on FR4 Board, t < 10 sec.

- **Package Information**



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