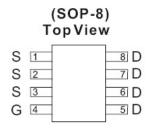


30V P-Channel Enhancement Mode MOSFET

Features

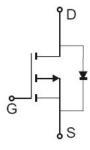
1.-30V/-5.3A, RDS(ON)_{TYP}=45m Ω @VGS=-10V 2.-30V/-4.2A, RDS(ON)_{TYP}=65m Ω @VGS=-4.5V

Pin Configurations



General Description

The FS9435 is the P-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.



● Absolute Maximum Ratings @T_A=25°C unless otherwise noted

Absolute Maximum Ratings (T _A =25	Unless Otherwi	ise Noted)		
Parameter		Symbol	Limits	Units
Drain-Source Voltage		V _{DS}	-30	V
Gate-Source Voltage		V _{GS}	20	V
Continuous Drain Current		ID	-5.3	A
Pulsed Drain Current ¹⁾		I _{DM}	-20	A
Maximum Power Dissipation	T _A =25	P _D	2.5	w
	T _A =70			VV
Operating Junction Temperature		TJ	-55 to 150	${\mathbb C}$
Junction-to-Case Thermal Resistance		R _{JC}	30	/W
Junction-to-Ambient Thermal Resistance (PCB mounted) ²⁾		R _{JA}	50	W

Notes

- 1.Maximum DC current limited by the package
- 2.1-in² 2oz Cu PCB board

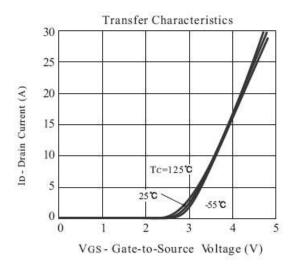
● Electrical Characteristics @T_A=25°C unless otherwise noted

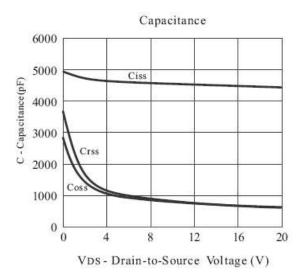
Symbol	Parameter	Conditions	Min	Тур	Max	Units
		Static			•	
B _{VDSS}	Drain-Source Breakdown Voltage	V _{GS} =0V,I _D =-250 A	-30			V
R _{DS(ON)} Drain-Source On-Resis	Brain Course On Besistance	V _{GS} = -10V, I _D = -5.3A		45	55	- mΩ
	Drain-Source On-Resistance	V _{GS} =-4.5V, I _D = -4.2A		65	75	
V _{GS(th)}	Gate-Threshold Voltage	V _{GS} =VGS, I _D =-250 A	-1.0	-2.2	-3.0	V
I _{GSS}	Gate-Body Leakage	V _{GS} =+20V, V _{DS} = 0V			+100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24V, V _{GS} = 0V			-1	Α
g FS	Forward Transconductance	$V_{DS} = -15V, I_{D} = -5.3A$	4	7		S
		Dynamic				
Q_g	Total Gate Charge			9.52		
Q_{gs}	Gate-Source Charge	V _{DS} =-15V, ID=-5.3A, V _{GS} =-10V		3.43		nC
Q_{gd}	Gate-Drain Charge			1.71		
t _{D(on)}	Turn-On Delay Time			34.5		
t _r	Turn-On Rise Time	V_{DD} = -15V, R_L = 15 I_D = -1A,		18.6		
t _{D(off)}	Turn-Off Delay Time	V_{GEN} =-10V R_G = 6 37.1		37.1		ns
t _f	Turn-Off Fall Time					

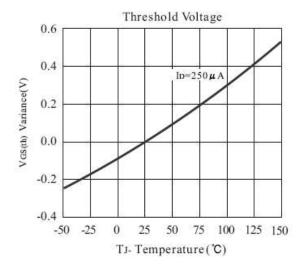
Notes:

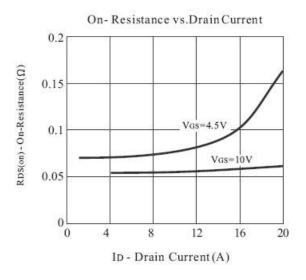
- 1. Pulse width limited by maximum junction temperature. Pulse test: $P_W \leqslant 300~\mu$ s, duty cycle $\leqslant 2\%$.
- 2. For design AID only, not subject to production testing. Switching time is essentially independent of operating temperature.

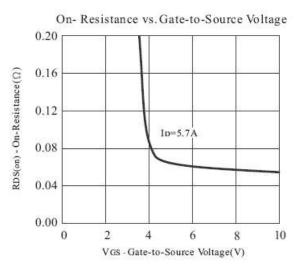
Typical Performance Characteristics

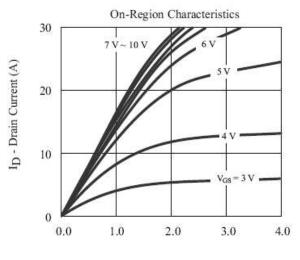










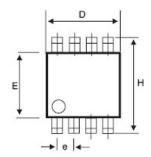


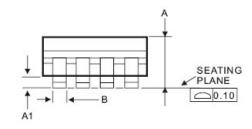
V_{DS} - Gate-to-Source Voltage (V)

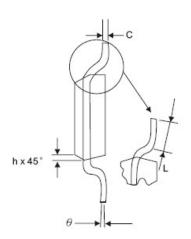
Package Information

Physical Dimensions inches(millimeters) unless otherwise noted

SOP-8







DIM	MILLIMETERS				
	MIN	MAX			
Α	1.35	1.75			
A1	0.10	0.25			
В	0.35	0.49			
С	0.18	0.25			
D	4.80	5.00			
Е	3.80	4.00			
е	1.27 BSC				
Н	5.80	6.20			
h	0.25	0.50			
L	0.40	1.25			
θ	0°	7°			

IMPORTANT NOTICE

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