

-100V P-Channel MOSFET

Features

-100V/-18A,

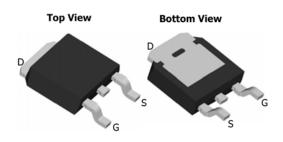
 $R_{DS(ON)}$ <100m Ω @ V_{GS} = - 10V Lead Free Available (RoHS Compliant)

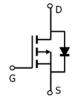
General Description

The FS2245 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. this device is well suited for high current load applications.

• Pin Configuration







TO252

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V _{DS}	-100	V	
Gate-Source Voltage		V _{GS}	±20	7	
Continuous Drain Current	T _A =25°C		-18	А	
	T _A =70°C	I _D	-12		
Pulsed Drain Current note		I _{DM}	-72	7	
Avalanche energy L=1mH note		E _{AS} , E _{AR}	722	mJ	
Power Dissipation note	T _A =25°C	D	50	w	
	T _A =70°C	→ P _D	25		
Junction and Storage Temperature Range		T _J , T _{STG}	-55 to 150	°C	

Thermal Characteristics								
Parameter		Symbol	Тур	Max	Units			
Maximum Junction-to-Ambient ^A	t ≤ 10s	Б	17	26				
Maximum Junction-to-Ambient AD	Ctoody Ctoto	$R_{ hetaJA}$	40	50	°C/W			
Maximum Junction-to-Lead	Steady-State	R _{θJL}	2.5	3				

Note:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, $t \leqslant 10$ sec. Pulse Test: Pulse Width $\leqslant 300\,\mu$ s, Duty Cycle $\leqslant 2\%$.
- 3. EAS condition: Tj=25 $^{\circ}$ C,VDD=-30V,VG=-10V,L=1mH,Rg=25 $^{\circ}$ Q,IAS=38A

• Electrical Characteristics (T_A=25°C unless otherwise noted)

Symbol	Parameter	Condition	Conditions		Тур	Max	Units	
STATIC PA	ARAMETERS							
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	I _D =-250μA, V _{GS} =0V				V	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-100V, V _{GS} =0	T _A =25°C		-0.002	-1	uA	
		V _{DS} 100V, V _{GS} -0	T _A =55°C			-5		
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V				±0.1		
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =VGS I _D =-250µ	V _{DS} =VGS I _D =-250µA		-1.9	-3.0	V	
I _{D(ON)}	On state drain current ^{note}	V _{GS} =-10V, V _{DS} =-5V	V _{GS} =-10V, V _{DS} =-5V				Α	
D	Otatia Dania Cauran On Besintan	V _{GS} =-10V, I _D =-20A	T _A =25°C		85	100	0	
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-4.5V, I _D =-10A		-			mΩ	
g _{FS}	Forward Trans conductance	V _{DS} =-10V, I _D =-20A	V _{DS} =-10V, I _D =-20A		25		S	
V _{SD}	Diode Forward Voltage	I _S =-1A,V _{GS} =0V	I _S =-1A,V _{GS} =0V		-0.75	-1.2	V	
Is	Maximum Body-Diode Continuous Curr	ent	t			-12	Α	
DYNAMIC	PARAMETERS			•			•	
C _{iss}	Input Capacitance		V _{GS} =0V, V _{DS} =-30V, f=1MHz		2460		pF	
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =-30V, f			615			
C _{rss}	Reverse Transfer Capacitance				246			
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz			6	10	Ω	
SWITCHIN	IG PARAMETERS			•			•	
Q _g (10V)	Tatal Oats Observe				55.5		nC	
Q _g (4.5V)	Total Gate Charge				35			
Q _{gs}	Gate Source Charge	V_{GS} =-10V, V_{DS} =-30V	V _{GS} =-10V, V _{DS} =-30V, I _D =-12A		16			
Q _{gd}	Gate Drain Charge				19			
t _{D(on)}	Turn-On Delay Time				15			
t _r	Turn-On Rise Time	V _{GS} =-10V, V _{DS} =-30V	V_{GS} =-10V, V_{DS} =-30V, R_L =2.5 Ω ,		17		ns	
t _{D(off)}	Turn-Off Delay Time	R_{GEN} =3 Ω			40			
t _f	Turn-Off Fall Time				45			
t _{rr}	Body Diode Reverse Recovery Time	I _F =-12A, dI/dt=100A/	I _F =-12A, dI/dt=100A/μs		50	65		
Qrr	Body Diode Reverse Recovery Charge	I _F =-12A, dI/dt=100A/	I _F =-12A, dI/dt=100A/μs		59		nC	

A: The value of R_{BUA} is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The Power dissipation P_{DSM} is based on R_{BUA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ =175°C.

D. The R $_{\text{BJA}}$ is the sum of the thermal impedence from junction to case R $_{\text{BJC}}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μ s pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

^{*}This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

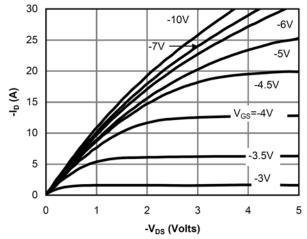


Fig 1: On-Region Characteristics

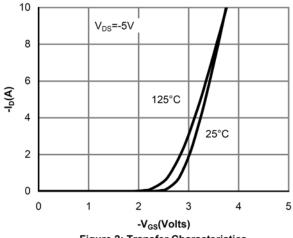


Figure 2: Transfer Characteristics

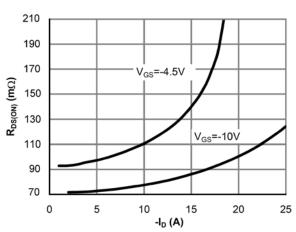


Figure 3: On-Resistance vs. Drain Current and **Gate Voltage**

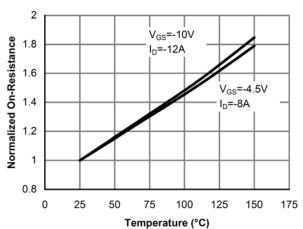


Figure 4: On-Resistance vs. Junction Temperature

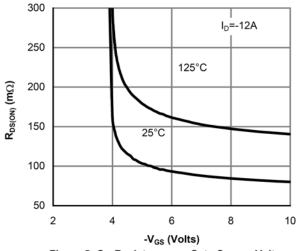


Figure 5: On-Resistance vs. Gate-Source Voltage

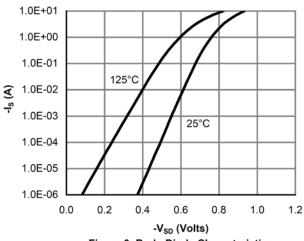
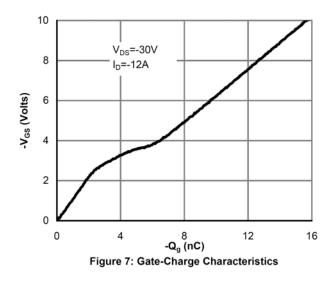


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



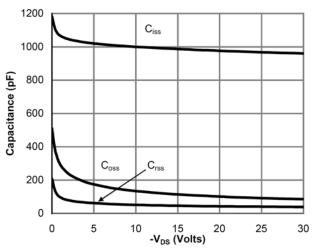


Figure 8: Capacitance Characteristics

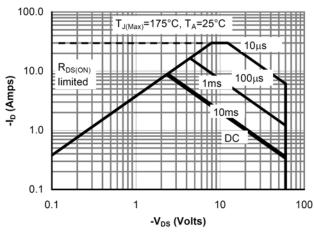


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

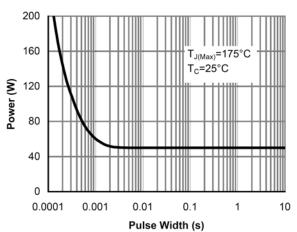


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

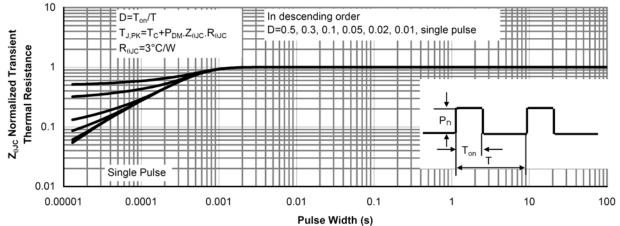


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

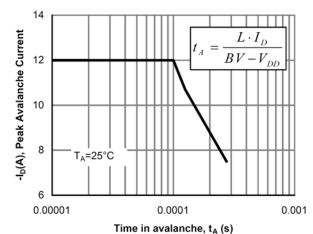


Figure 12: Single Pulse Avalanche capability

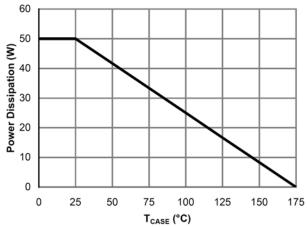


Figure 13: Power De-rating (Note B)

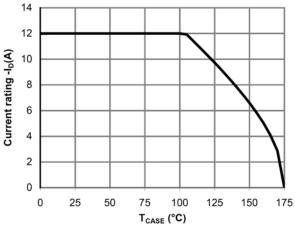


Figure 14: Current De-rating (Note B)

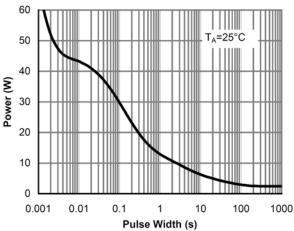


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

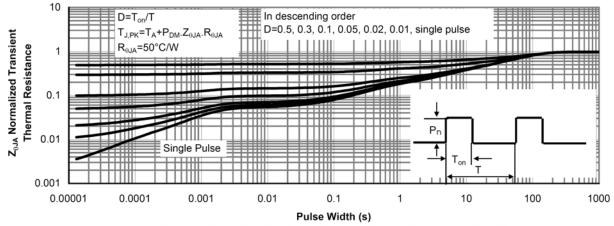
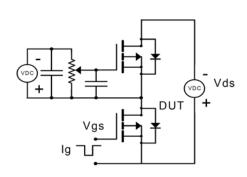
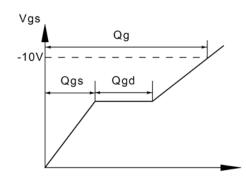


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

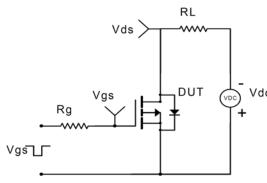
FS2245

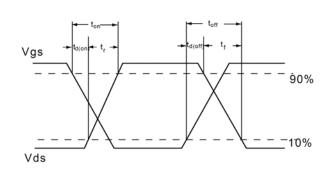
Gate Charge Test Circuit & Waveform



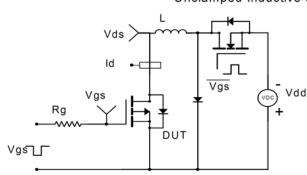


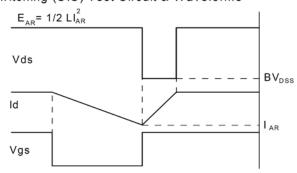
Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms

