

N-Channel Enhancement Mode Field Effect Transistor

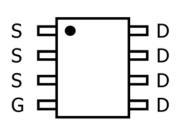
Features

- N-channel, normal leve
- Very low on-resistance R_{DS(on)}
- 150 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC for target application
- Ideal for high-frequency switching and synchronous rectification

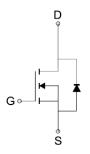
Product Summary

V_{DS}	V_{GS}	Test Conditions	R _{DS(on)}
60V	±20V	5A@VGS=10V	35mR
		4.5A@ VGS=4V5	40mR

• Pin Configurations(TO252)







N-Channel MOSFET

Absolute Maximum Ratings TA=25°C unless otherwise noted

Parameter			Ratings	Unit
Drain-Source Voltage		V _{DSS}	60	V
Gate-Source Voltage		V _{GSS}	±20	V
Drain Current	Continuous	I _D	5 ^(1A) 20 ^(1B)	А
	Pulse	I _{DM}	60	
Total Power Dissipation (note1)		P _D	0.8 ^(1A)	w
		D	25 ^(1B)	**
Operating and Storage Junction Temperature Range		T_{J}, T_{STG}	-55 to +150	°C

Notes

- 1A. Surface Mounted on 1x1FR4 Board.
- 2. The value of PD is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The value in any given application depends on the user's specific board design. The current rating is based on the DC thermal resistance rating and PCB layout: A. Minimum footprint; B. With additional heat sink.
- 3. Repetitive rating, pulse width limited by junction temperature

• Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter (note2)	Symbol	Test Conditions	Min	Тур	Max	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 uA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA
Gate-Body Leakage	l _{GSS}	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA
Gate Threshold Voltage	V _{GS(TH)}	$V_{DS} = V_{GS}, I_{D} = 250 \text{ uA}$	1	1.4	3	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10 V, I _D = 5.0 A		35	41	mR
		V _{GS} = 4.5 V, I _D = 4.5 A		40	55	
Input Capacitance	C _{ISS}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V},$		1180		pF
		F = 1MHz				
Output Capacitance	C _{oss}			170		
Reverse Transfer Capacitance	C _{RSS}			100		
Turn-On Delay Time	T _{D(ON)}	V _{GS} =10V, V _{DS} =30V,			25	nS
		R _L =5.4R,				
		R_{GEN} =3R, I_D =5.5A				
Turn-On Rise Time	T _R				70	
Turn–Off Delay Tim	T _{D(OFF)}				300	
Turn–Off Fall Time	T _F				150	
Diode Forward Voltage	V _{SD}	$V_{GS} = 0 \text{ V, I}_{S} = 2 \text{ A}$	0.5	0.77	1.0	V

^{1.} The value of PD is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The value in any given application depends on the user's specific board design. The current rating is based on the DC thermal resistance rating and PCB layout: A. Minimum footprint; B. With additional heat sink.

^{2.} Repetitive rating, pulse width limited by junction temperature

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

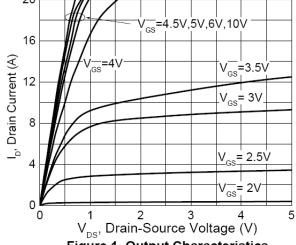


Figure 1. Output Characteristics

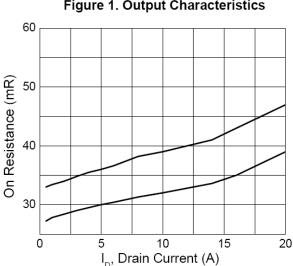


Figure 3. On-Resistance

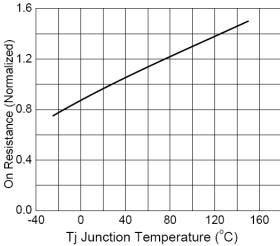
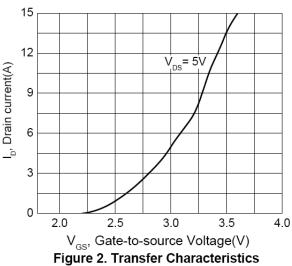


Figure 5 . On-Resistance vs. Temperature



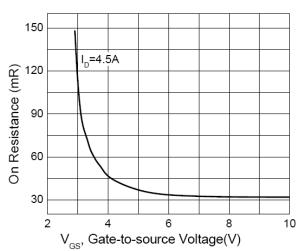


Figure 4. On-Resistance vs. Threshold Voltage

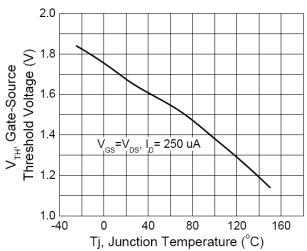
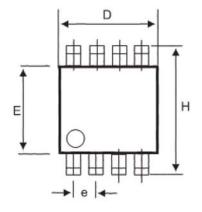
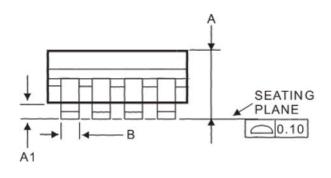


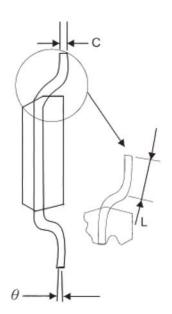
Figure 6. Gate Threshold Vs. Temperature

• Package Information

SOP-8 Package Outline







DIM	MILLIMETERS (mm)		
DIM	MIN	MAX	
Α	1.35	1.75	
A1	0.10	0.25	
В	0.35	0.49	
С	0.18	0.25	
D	4.80	5.00	
E	3.80	4.00	
е	1.27 BSC		
Н	5.80	6.20	
L	0.40	1.25	
θ	0°	7 °	

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.