

N-Channel Enhancement Mode Field Effect Transistor

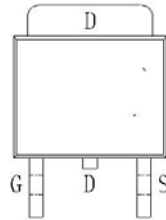
Features

- N-channel, normal level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC for target application
- Ideal for high-frequency switching and synchronous rectification

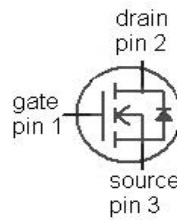
Product Summary

V_{DS}	200	V
$R_{DS(on),max}$ (TO252)	180	mΩ
$(I_{DM})^b$	20	A

Pin Configurations(TO252)



Top View



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V_{DS}	200	V	
Gate-Source Voltage		V_{GS}	±30		
Continuous Drain Current($T_J=150^\circ\text{C}$) ^a	$T_A=25^\circ\text{C}$	I_D	20	A	
	$T_A=100^\circ\text{C}$		12		
Pulsed Drain Current ^b		I_{DM}	60		
Avalanche Current ^b	L=0.1mH	I_{AS}	65		
Avalanche energy		E_{AS}	17	mJ	
Power Dissipation ^a	$T_A=25^\circ\text{C}$	P_D	65	W	
	$T_A=70^\circ\text{C}$		50		
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C	
Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^a	$t \leq 5\text{s}$	$R_{\theta JA}$	78	100	°C/W
	Steady-State		120	150	
Maximum Junction-to-Lead		$R_{\theta JL}$	40	50	

Notes

a. Surface Mounted on 1x1FR4 Board.

b. Pulse width limited maximum junction temperature Pulse test: $PW \leq 300 \mu\text{s}$ duty cycle $\leq 2\%$

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● Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=1\text{mA}, V_{GS}=0\text{V}$	200			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=200\text{V}, V_{GS}=0$			10	uA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 30\text{V}$			± 0.1	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2		4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ^a	$V_{GS}=10\text{V}, I_D=10\text{A}$		140	180	mΩ
g_{FS}	Forward Trans conductance ^a	$V_{DS}=15\text{V}, I_D=10\text{A}$	7	13		S
V_{SD}	Diode Forward Voltage	$I_S=13\text{A}, V_{GS}=0\text{V}$	0.3		1.2	V
I_S	Maximum Body-Diode Continuous Current				3	A
Dynamic^b						
C_{iss}	Input capacitance	$V_{GS}=0\text{V}, V_{DS}=50\text{V}, f=1\text{MHz}$		830	1080	pF
C_{oss}	Output capacitance			200	260	
C_{riss}	Reverse transfer capacitance			25	33	
Q_g	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=160\text{V}, I_D=13\text{A}, R_G=2.4\ \Omega$		20	26	nC
Q_{gs}	Gate - Source Charge			5.3		
Q_{gd}	Gate - Drain Charge			10		
R_g	Gate resistance		0.5		2.5	
Switching						
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DS}=160\text{V}, R_L=30\ \Omega, R_{GEN}=2.4\ \Omega, I_D=13\text{A}$		9	13	ns
t_r	Turn-On Rise Time			4	6	
$t_{D(off)}$	Turn-Off Delay Time			13	18	
t_f	Turn-Off Fall Time			3	4	
t_{rr}	Body Diode Reverse Recovery Time		$I_F=3\text{A}, dI/dt=100\text{A}/\mu\text{s}$		67	

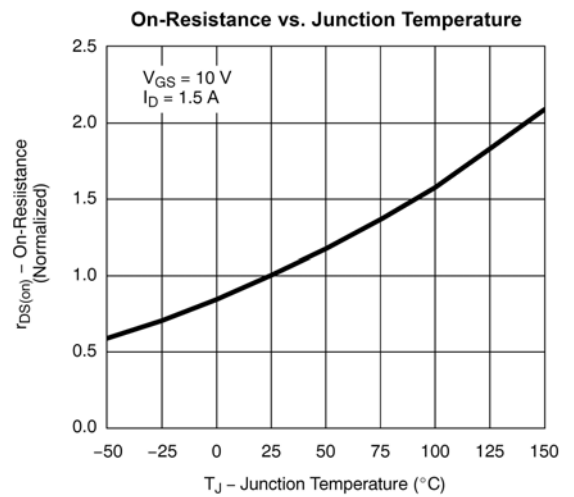
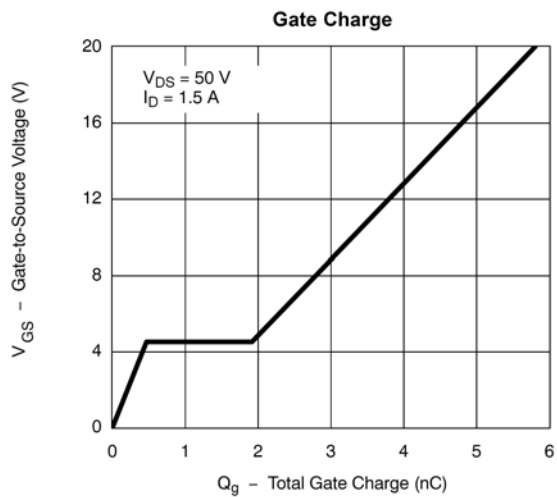
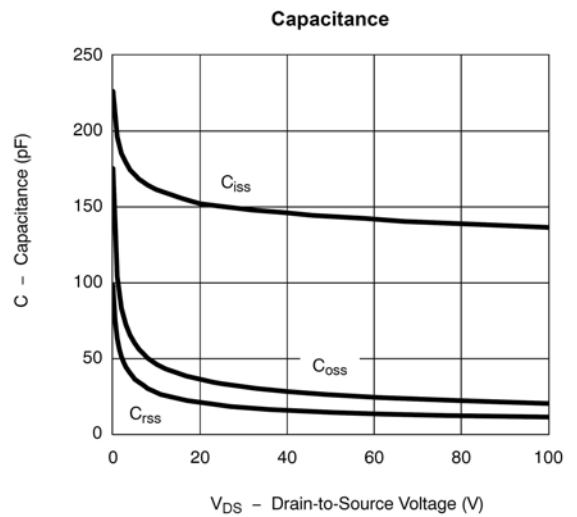
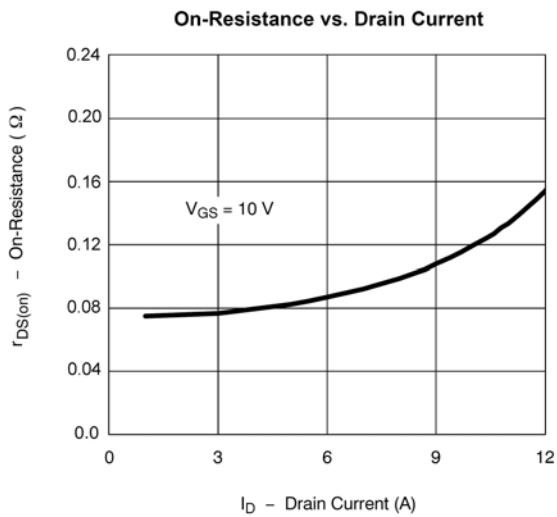
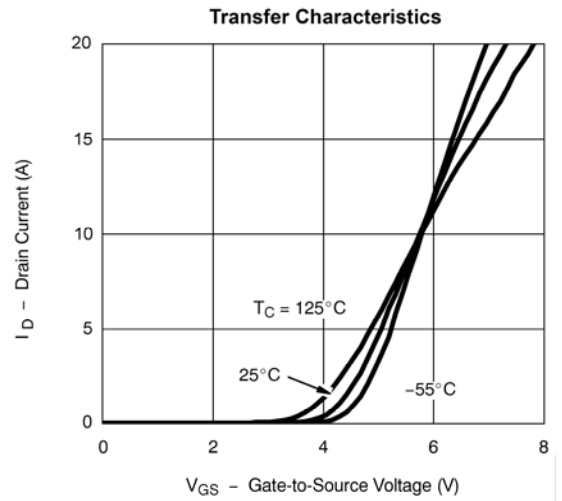
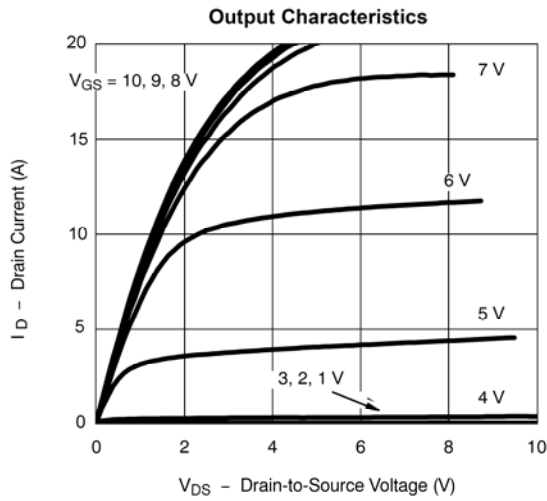
Notes

a. Pulse test: $PW \leq 300\ \mu\text{s}$ duty cycle $\leq 2\%$

b. Guaranteed by design, not subject to production testing.

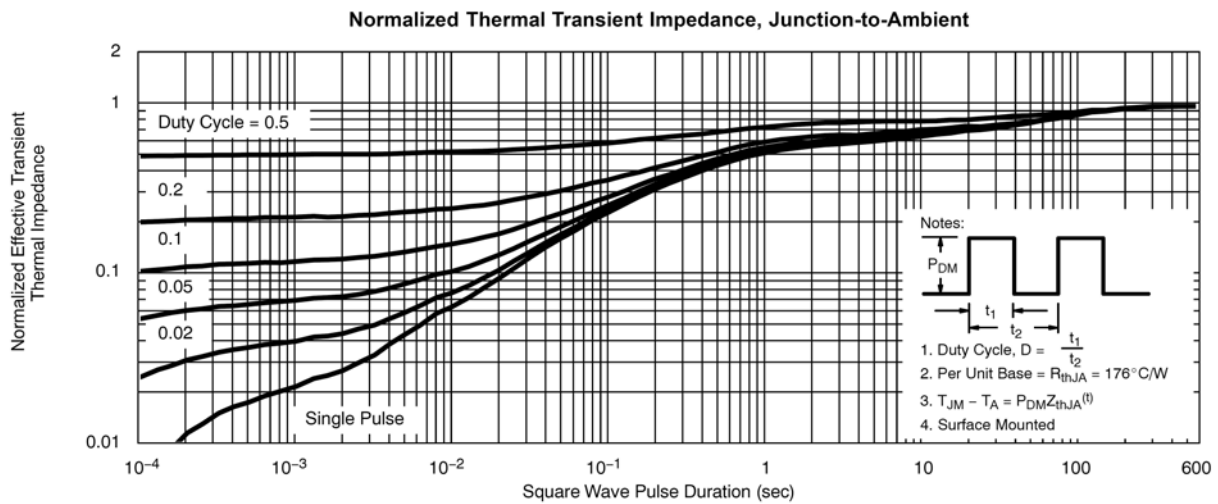
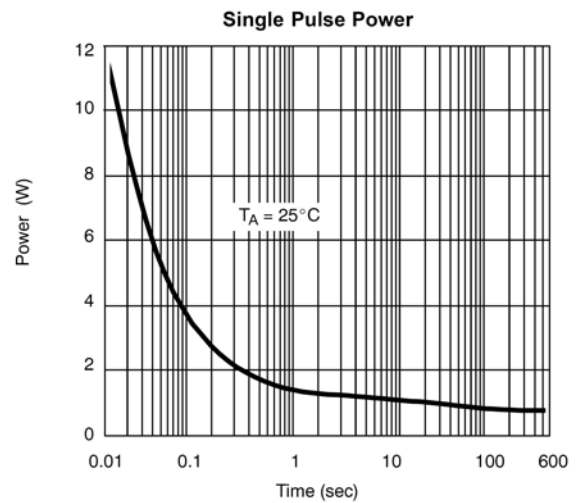
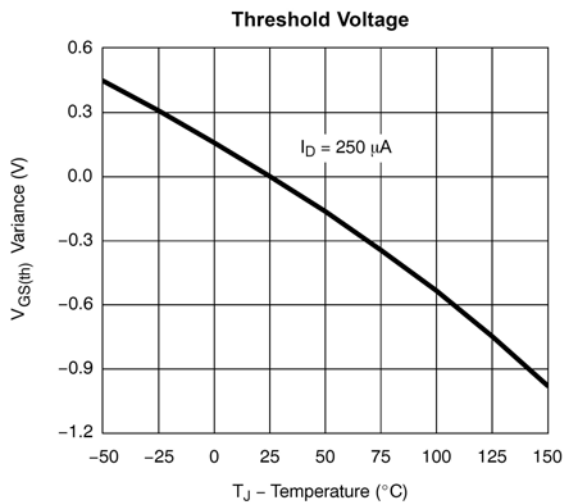
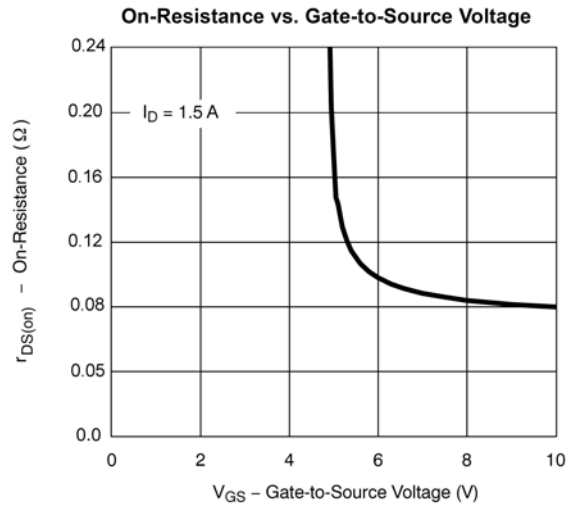
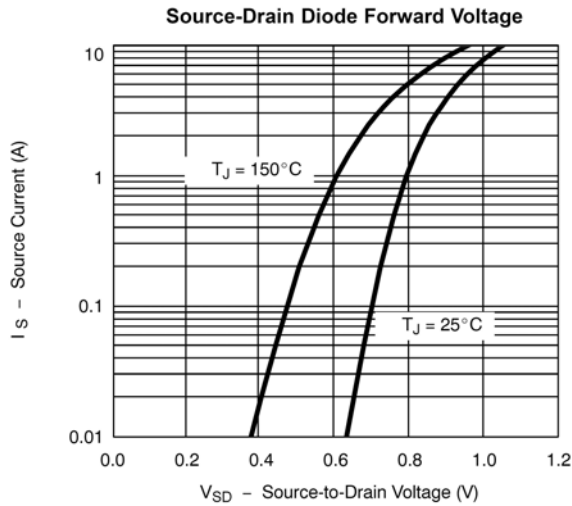
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TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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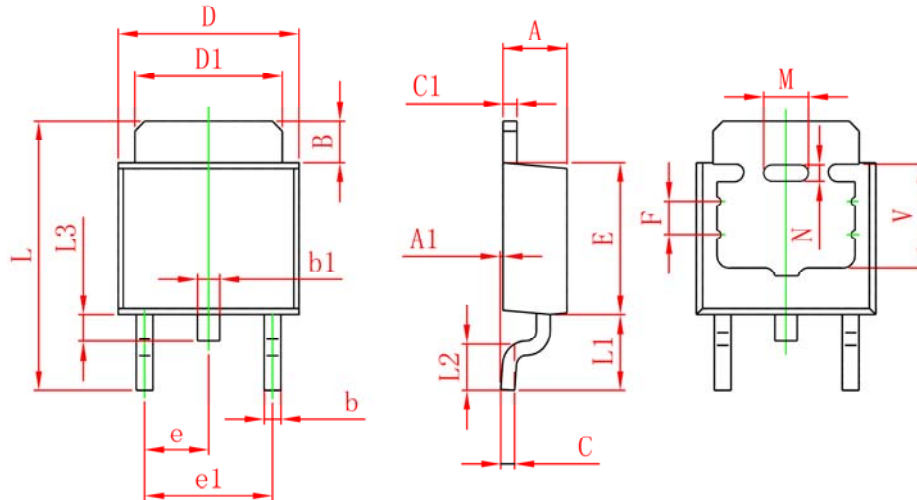
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- Package Information

TO-252C-2L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
F	1.200REF.		0.047REF.	
M	1.600REF.		0.063REF.	
N	0.450REF.		0.018REF.	
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.600	0.900	0.024	0.035
V	3.800 REF		0.150 REF	