800KHz 1.1A Synchronous Boost DC/DC Regulator

Features

Up to 96% Efficiency
Delivers 100mA@3.3V from Single AA Cell
Delivers 300mA@5V from Two AA Cells
Delivers 600mA@5V from Single Li Cell
Low Voltage Start-Up: 0.85V
800KHz Fixed Frequency Switching
Input Range: 0.9V to5V
Output Range:2.5V to 4.5V (Up to 5V with Schottky)
Logic Controlled Shutdown(<1μA)
Anti-ringing Control Minimizes EMI
1.1A Peak Switch Current Limit
Over Temperature Protection

Applications

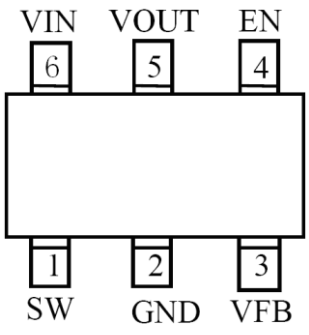
Digital Still and Video Cameras
Personal Information Appliances
Wireless and DSL Modems
Personal Medical Products
GPS Receivers
LCD Bias Supplies
Handheld Instruments
Portable Audio Players

General Description

The FS1703 devices provide a power supply solution for products powered by either a one-cell, two-cell, or three-cell alkaline, NiCd or NiMH, or one-cell Li-ion or Li-polymer battery. The boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using a synchronous rectifier to obtain maximum efficiency, which contains an internal NMOS switch and PMOS synchronous rectifier. The maximum peak current in the boost switch is typically limited to a value of 1.1A.

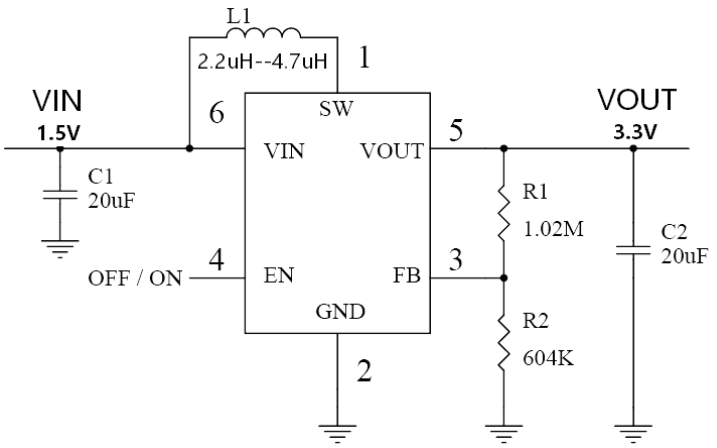
A switching frequency of 800KHz minimizes solution footprint by allowing the use of tiny, low profile inductors and ceramic capacitors. The current mode PWM design is internally compensated, reducing external parts count. Anti-ringing control circuitry reduces EMI concerns by damping the inductor in discontinuous mode. In shutdown, VOUT and VIN are connected, which allows the input battery to be used for backup power. The device features low shutdown current less than 1μA..

Pin Configurations



SOT23-6L

Typical Application Circuit



Absolute Maximum Ratings

Parameter		Symbol	Ratings	Unit
IN Pin Voltage		VIN	-0.3 to 7V	V
FB Pin Voltage		V_{FB}	-0.3 to 6V	V
EN Pin Voltage		V_{EN}	-0.3 to 7V	V
SW Pin Voltage		Vsw	-0.3 to 7V	V
Peak SW Sink Current		Iswmax	1.5	A
Power Dissipation		P_D	400	mW
Operating Junction Temperature		Topr	125	℃
Storage Temperature Range		Tstg	-40 to + 125	℃
Lead Temperature (Soldering, 10 seconds)		Tsolder	260	℃
ESD rating	Human Body Model	HBM	2000	V
	Machine Model	MM	200	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Caution

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. Chipower recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Recommended Operating Conditions

Parameter	Min.	Nom.	Max.	Units
Supply voltage at VIN	0.9	-	5.5	V
Output voltage at VOUT	2.5	-	5.5	V
Operating free air temperature range(1), TA	-40	-	85	℃
Operating virtual junction temperature range, Tj	-40	-	125	℃

Electrical Characteristics

(VIN=1.2V,TA= 25℃ Vout=3.3V C1=C2=20uF all capacitors are ceramic, unless otherwise specified.)

Parameter	Conditions	Min	Typ(1)	Max	Units
Output Voltage Range (Adj.) (3)		2.5		5	V
Minimum Start-Up Voltage	I_{LOAD} =1mA		0.85	1	V
Minimum Operating Voltage(2)	EN = VIN		0.5	0.65	V
Switching Frequency			800		KHz
Max Duty Cycle	V_{FB} = 1.15V	80	87		%
Current Limit Delay to Output			40		ns
Feedback Voltage		1.192	1.23	1.268	V
Feedback Input Current(4)	V_{FB} = 1.3V		30		nA
NMOS Switch Leakage	V_{SW} =5V		0.1	5	μA
PMOS Switch Leakage	V_{SW} =0V		0.1	5	μA
NMOS Switch On Resistance(5)	V_{OUT} = 3.3V		0.35		Ω
	V_{OUT} = 5V(6)		0.2		
PMOS Switch On Resistance(5)	V_{OUT} = 3.3V		0.45		Ω
	V_{OUT} = 5V(6)		0.3		
NMOS Current Limit(7)	VIN=2.5V		1100		mA
Quiescent Current (Active)	Measured On VOUT, Non-switching		300	500	μA
Shutdown Current	V_{EN}=0V, Including Switch Leakage		0.1	1	μA
En Input High(8)		1.5			V
En Input Low(9)				0.35	V
En Input Current	V_{EN} = 5.5V		0.01	1	μA

(1) Typical numbers are at 25°C and represent the most likely norm.

(2) Minimum VIN operation after start-up is only limited by the battery's ability to provide the necessary power as it enters a deeply discharged state.

(3) The fixed voltage version effective output voltage.

(4) Bias current flows into FB pin. Specification is guaranteed by design and not 100% tested in production.

(5) Does not include the bond wires. Measured directly at the die.

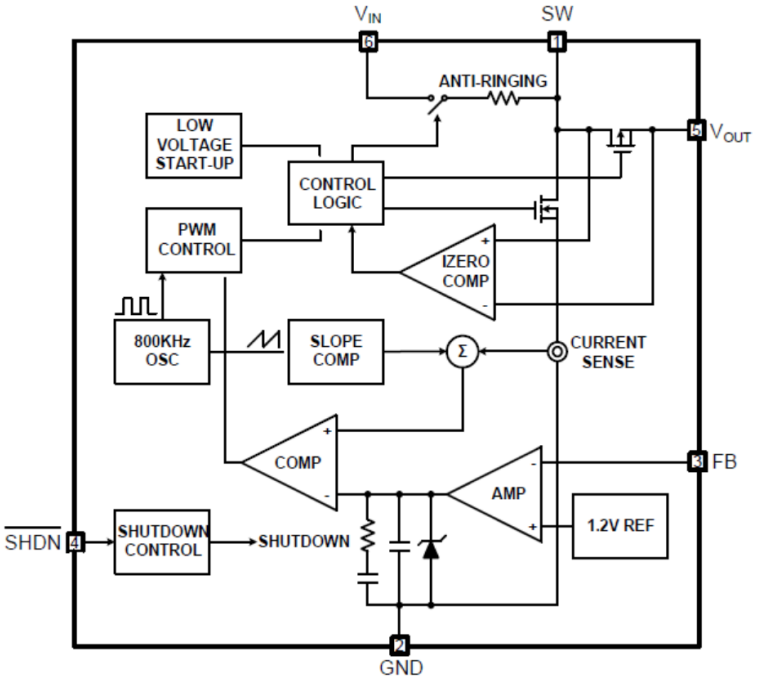
(6) Specification is guaranteed by design and not 100% tested in production.

(7) Duty cycle affects current limit due to ramp generator.

(8) High Voltage level：Forcing EN above 1.5V enables the part.

(9) Low Voltage level：Forcing EN below 0.35V shuts down the device. In shutdown, all functions are disabled drawing <1 μA supply current. Do not leave EN floating.

- **Typical Block Diagram**



- **Pin Description**

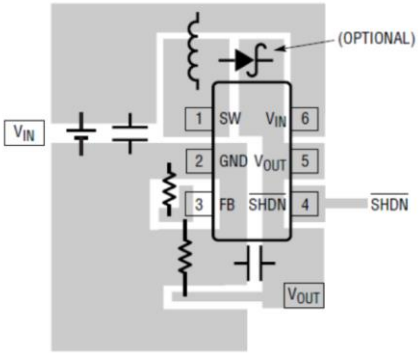
Pin Port	Pin Name	Pin Description
①	**SW**	**Switch Pin.**Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot. If the inductor current falls to zero, or CE is low, an internal 100Ω antiringing switch is connected from SW to VIN to minimize EMI.
②	**GND**	**Signal and Power Ground**. Provide a short direct PCB path between GND and the (–) side of the output capacitor(s). Connect GND with large copper areas directly to the input and output supply returns and negative terminals of the input and output capacitors.
③	**FB**	**Feedback Input / Not Connected** (for fixed output voltage option). The output voltage can be adjusted from 2.5V to 5.5V by: VOUT =1.23V•[1+(R1/R2)] The feedback networks should be connected directly to a dedicated analog ground plane and this ground plane must connect to the GND pin. If no analog ground plane is available, then the ground connection of the feedback network must tie directly to the GND pin. The feedback network, resistors R1 and R2 must be connected to FB pin directly as closely as possible. And FB is a sensitive signal node, trace area at FB pin should be small. Please keep FB away from the inductor and SW switching node on the PCB layout to minimize copper trace connections that can inject noise into the system.
④	**EN**	**Logic Controlled Shutdown Input.** EN = High: Normal free running operation, 1.4MHz typical operating frequency. EN = Low: Shutdown, quiescent current <1μA. Output capacitor can be completely discharged through the load or feedback resistors.
⑤	**VOUT**	**DC-DC Power Output** (Drain of the Internal Synchronous Rectifier P-MOSFET) and Output

		Voltage Sense Input. Bias is derived from VOUT when VOUT exceeds 2.3V. PCB trace length from VOUT to the output filter capacitor(s) should be as short and wide as possible. Care should be taken to minimize the loop area formed by the output filter capacitor(s) connections, the VOUT pin, and the FS1703 GND pin. The minimum recommended output filter capacitance is 4.7µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VOUT pin and the GND pin. VOUT is held at approximately VIN – 0.6V in shutdown due to the body diode of the internal PMOS.
⑥	**IN**	**Battery Supply Input Voltage**. The device gets its start-up bias from VIN. Once VOUT exceeds VIN, bias comes from VOUT. Thus, once started, operation is completely independent from VIN. Operation is only limited by the output power level and the battery's internal series resistance. The VIN pin should be connected to the positive terminal of the battery and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the FS1703 GND pin. The minimum recommended bypass capacitance is 1µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pin and the GND pin. PCB trace length from VIN to the input filter capacitor(s) should be as short and wide as possible.

- **Application note:**

PCB LAYOUT GUIDELINES

The high speed operation of the FS1703 demands careful attention to board layout. You will not get advertised performance with careless layout. The followed figure shows the recommended component placement. A large ground pin copper area will help to lower the chip temperature. A multilayer board with a separate ground plane is ideal, but not absolutely necessary.



Recommended Component Placement for Single Layer Board

INDUCTOR SELECTION

The FS1703 can utilize small surface mount and chip inductors due to its fast 800KHz switching frequency. Typically, a 2.2µH ~4.7µH inductor is recommended for most applications. Larger values of inductance will allow greater output current capability by reducing the inductor ripple current. Increasing the inductance above 10µH will increase size while providing little improvement in output current capability.

$$I_{OUT(MAX)} = \eta \bullet \left(I_P - \frac{V_{IN} \bullet D}{f \bullet L \bullet 2}\right) \bullet (1-D)$$

where:

η= estimated efficiency

I_P = peak current limit value (1.1A)

V_{IN} = input (battery) voltage

D = steady-state duty ratio = (VOUT – VIN)/VOUT

f = switching frequency (800KHz typical)

L = inductance value

The inductor current ripple is typically set for 20% to 40% of the maximum inductor current (IP). High frequency ferrite core inductor materials reduce frequency dependent power losses compared to cheaper powdered iron types, improving efficiency. The inductor should have low ESR (series resistance of the windings) to reduce the I^2R power losses, and must be able to handle the peak inductor current without saturating. Molded chokes and some chip inductors usually do not have enough core to support the peak inductor currents of 850mA seen on the FS1703. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor. See Table 1 for some suggested components and suppliers.

Table 1. Recommended Inductors

Part Number	Value (μH)	Max DCR (mΩ)	Rated DC Current(A)	Size W×L×H (mm)
Sumida	**2.2**	**75**	**1.20**	
CDRH	**3.3**	**110**	**1.10**	**3.8×3.8×1.8**
3D16	**4.7**	**162**	**0.90**	
Sumida	**2.2**	**71.2**	**1.75**	
CR43	**3.3**	**86.2**	**1.44**	**4.3×4.8×3.5**
	4.7	**108.7**	**1.15**	
Sumida	**2.2**	**75**	**1.32**	
CDRH	**3.3**	**110**	**1.04**	**4.7×4.7×2.0**
4D18	**4.7**	**162**	**0.84**	

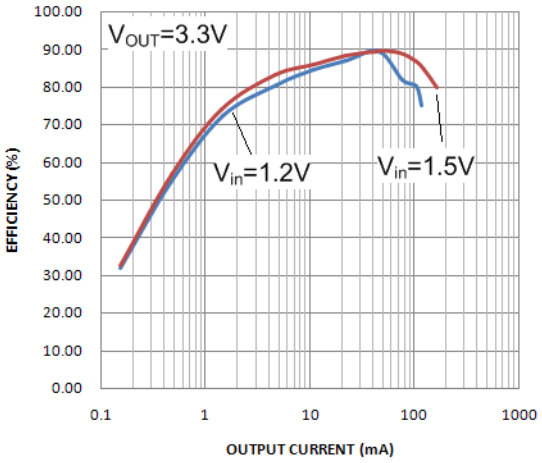
OUTPUT AND INPUT CAPACITOR SELECTION

Low ESR (equivalent series resistance) capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have extremely low ESR and are available in small footprints. A 4.7μF to 20μF output capacitor is sufficient for most applications. Larger values up to 22μF may be used to obtain extremely low output voltage ripple and improve transient response. An additional phase lead capacitor may be required with output capacitors larger than 10μF to maintain acceptable phase margin. X5R and X7R dielectric materials are preferred for their ability to maintain capacitance over wide voltage and temperature ranges.

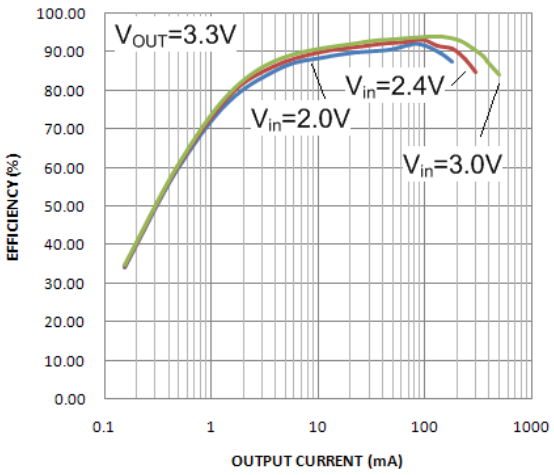
Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. It follows that ceramic capacitors are also a good choice for input decoupling and should be located as close as possible to the device. A 10μF input capacitor is sufficient for virtually any application. Larger values may be used without limitations. Table 2 shows a list of several ceramic capacitor manufacturers. Consult the manufacturers directly for detailed information on their entire selection of ceramic capacitors.

- **Typical Performance Characteristics**

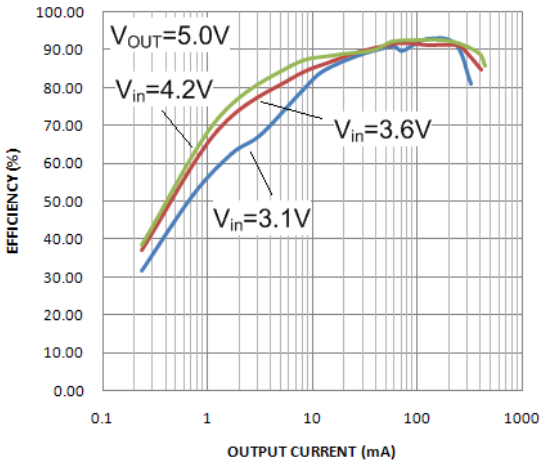
Efficiency vs Output Current



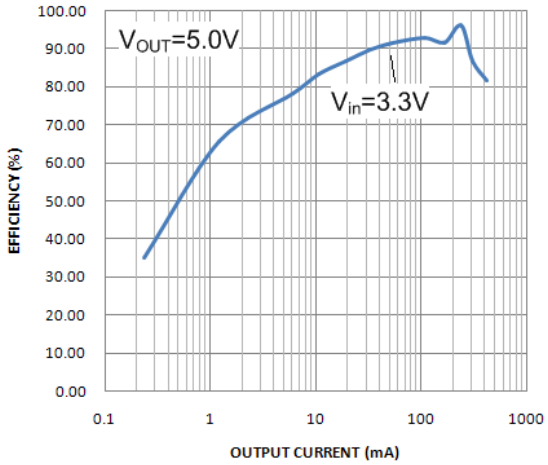
Efficiency vs Output Current



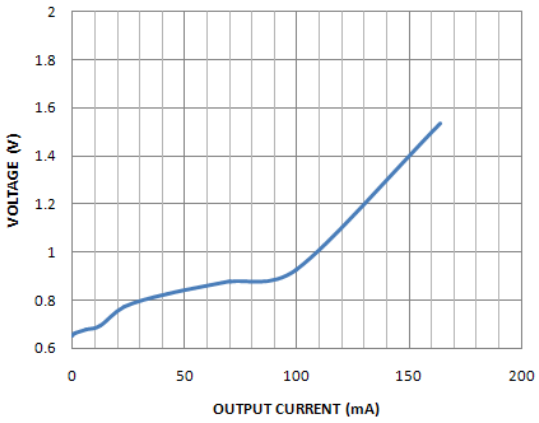
Efficiency vs Output Current



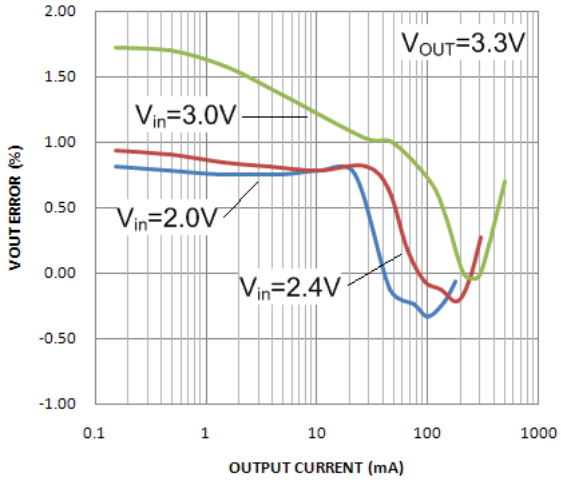
Efficiency vs Output Current



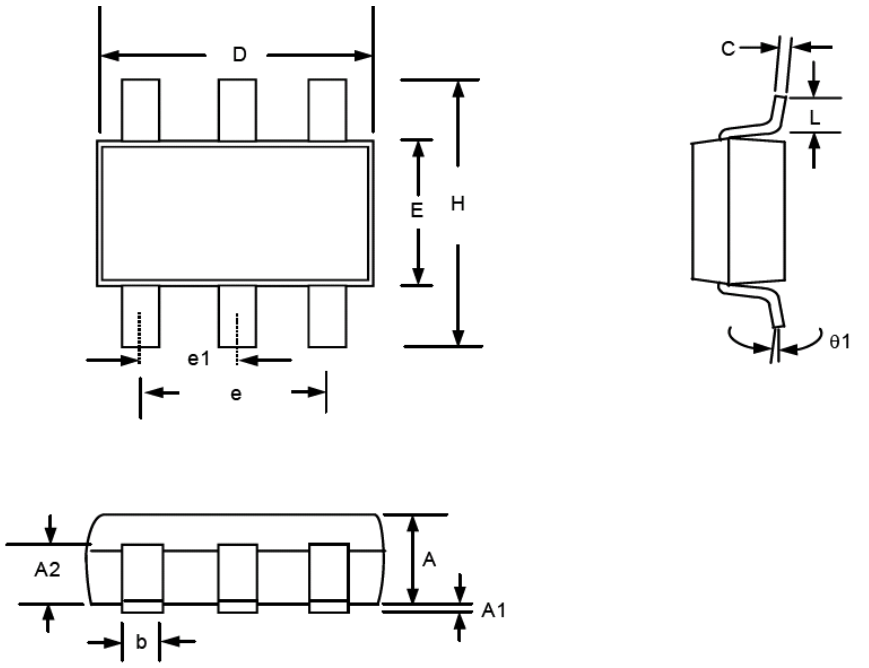
Minimum Start-Up Voltage vs Output Current



Load Regulation



- **Package Information**



Symbol	Dimension mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	1.00	1.10	1.30	0.039	0.043	0.051
A1	0.00		0.10	0.000		0.004
A2	0.70	0.80	0.90	0.028	0.031	0.035
b	0.35	0.40	0.50	0.014	0.016	0.020
C	0.10	0.15	0.25	0.004	0.006	0.010
D	2.70	2.90	3.10	0.106	0.114	0.122
E	1.40	1.60	1.80	0.055	0.063	0.071
e		1.90(TYP)			0.075(TYP)	
H	2.60	2.80	3.00	0.102	0.110	0.118
L	0.37			0.015		
θ1	1º	5º	9º	1º	5º	9º